SQFlash SD Card Datasheet

(SQF-ISDx1-xG-D1x)

CONTENTS

Revision History

Rev.	Date	History
0.1	2018/12/14	1. 1st draft
0.2	2018/12/18	1. Update TBW data
0.3	2019/8/9	1. Update discussion

1. Overview

The Industrial SD Card (ISD) of the SQFlash is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions. Card capacities of non-secure area and secure area support [Part 3 Security Specification Ver4.00 Final] Specifications.

The SQF-ISD card has a 9-pin interface, designed to operate at a maximum frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. The Card capacity could be more than 32GB and up to 256GB in the future with ex-FAT file system, which is called SDXC (Extended Capacity SD Memory Card).

Secure Digital cards are one of the most popular cards today due to its high performance, good reliability and wide compatibility.

2. Standard Features

- **Support File system specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver4.0 Final] Specifications Support SD SPI mode**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **Non-UHS Mode**
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - **UHS Mode**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec

  NOTES: 1.Timing in 1.8V signaling is different from that of 3.3V signaling.
  2.To properly run the UHS mode, please ensure the device supports UHS-I mode.
- **The command list supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions**
- **Copyrights Protection Mechanism**
  - **Compliant with the highest security of DPRM standard**
- **Support CPRM (Content Protection for Recordable Media) of SD Card**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (optional)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **Electrostatic Discharge(ESD)**
  - **ESD protection in pads(contact discharge).**
  - **ESD protection in non-contact pad area(air discharge).**
- **Operation voltage range: 2.7 ~ 3.6V**
- **Support Dynamic and Static Wear Leveling**
- **Dimension : 32mm(L) x 24mm(W) x 2.1mm(H)**

3. Additional Features

■ Capacities

– 16GB，32GB，64GB，128GB，256GB

■ Flash type

– 3D TLC

■ Performance (MB per sec)

– Max. Read / Write: 95 / 85

■ Temperature Ranges

– Commercial Temperature
  - 0℃ to 70℃

– Industrial Temperature
  - -40℃ to 85℃

■ Mechanical Specification

– Shock：1500G, Peak / 0.5ms
– Vibration：80Hz~2000Hz/20G
– Drop Test: 1.5m free fall
– Torque Test: 0.1N-m or +/-2.5deg
– Switch Cycles Test: Slide 0.4N to 0.5N

■ Humidity

– Operating Humidity：RH = 95% under 25°C
– Non-Operating Humidity：RH = 95% under 40°C

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a flash drive can be written which is a measurement of flash drive's expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (Flash Drive Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 60,000 cycles
  - Ultra MLC: 20,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC (BiCS3): 3,000 cycles
- **Flash Drive Capacit**y: Physical capacity in total of a Flash Drive.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a flash drive controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

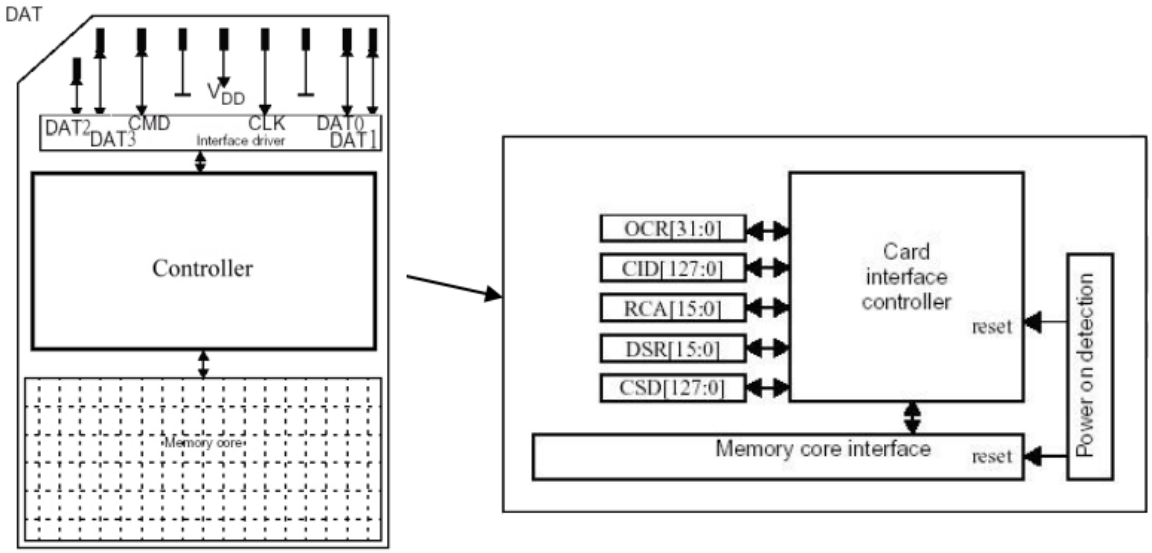
The TBW rating for a flash drive shall be derived for and verified under the following workload conditions,

- Sequential Write (copy file into card)
- P/E cycles incurred: erase count after writing – erase count before writing

➢ SQFlash SD Card TBW

	WAF	TBW
		3D TLC
16 GB	TBD	TBD
32 GB	1.0946	87
64 GB	1.0946	175
128 GB	1.0946	350
256 GB	1.0946	701

4. Pin Assignment and Block Diagram



SD memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	Type (1)	Description	Name	Type	Description
1	CD/DAT3 (2)	I/O/PP (3)	Card Detect/ Data Line[bit3]	CS	I (3)	Chip Select (net true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		
9	DAT2	I/O/PP	Data Line[bit2]	RSV		

(1) S: power supply, I:input; O:output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory**
OCR	32bit	Operation condition registers. **Mandatory**
SSR	512bit	SD Status; information about the card proprietary features. **Mandatory**
OCR	32bit	Card Status; information about the card status. **Mandatory**

RCA register is not used (or available) in SPI mode.

5. Performance Power Consumption

Table list as below is the power consumption of ISD card with different type of flash memory.

	Capacity	Specification	Performance		Power Consumption (Max)		
			TestMetrixTest @500MB		Read	Write	Standby
			Read(MB/s)	Write (MB/s)	(mA)	(mA)	(mA)
BiCS3	32GB	CL10, high reliability	95	15	400	400	1
	64GB	CL10, high reliability	95	25	400	400	1
	128GB	CL10, high reliability	95	25	400	400	1
	256GB	CL10, high reliability	95	25	400	400	1
	32GB	A1, V30, CL10	95	35	400	400	1
	64GB	A1, V30, CL10	95	65	400	400	1
	128GB	A1, V30, CL10	95	85	400	400	1
	256GB	A1, V30, CL10	95	85	400	400	1

NOTES:

(1) Power consumptions are measured at room temperature.

(2) Power Consumption may differ according to flash configuration, SDR configuration, or platform.

6. DC Characters

6.1 BUS Operating Conditions for 3.3V Signaling

Threshold level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	VOL		0.125*VDD	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25 *VDD	V	
Power up time			250	ms	From 0v to V_{DD}min.

Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Threshold Level for 1.8V Signaling

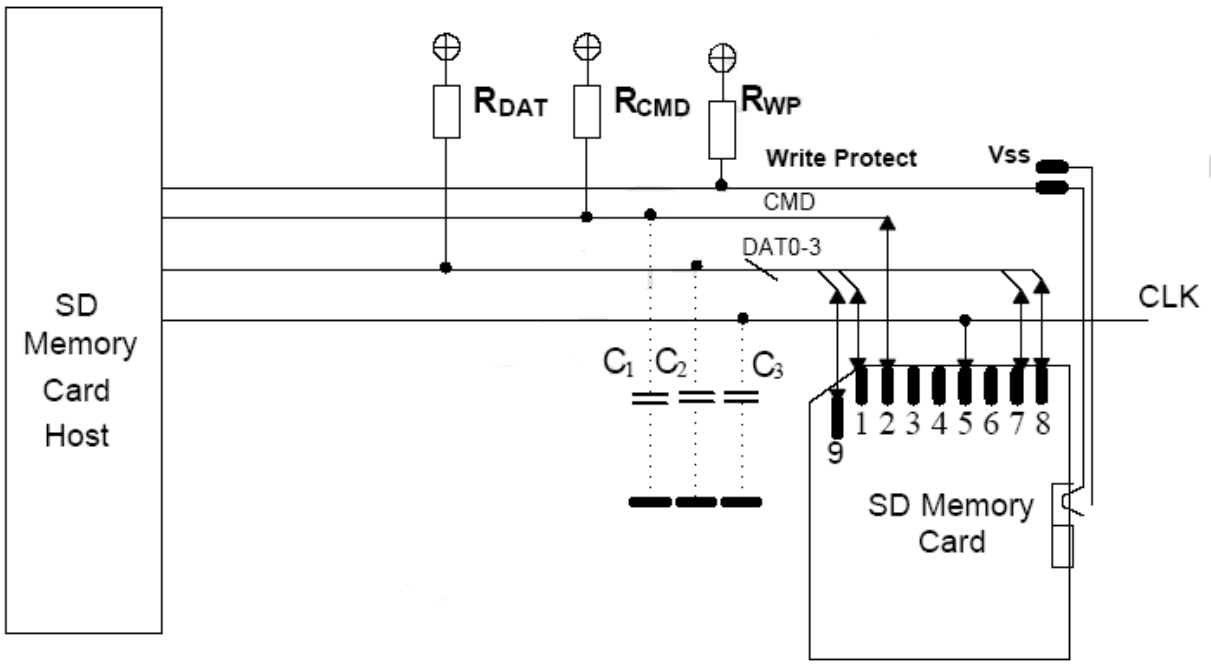
Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	VOH	1.4	-	V	IOH = -2mA
Output Low Voltage	VOL		0.45	V	IOL = 2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	V_{ss} – 0.3	0.58	V	

Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up isdisconnected.

6.2 BUS Operating Conditions for 3.3V Signaling

BUS Circuitry Diagram:



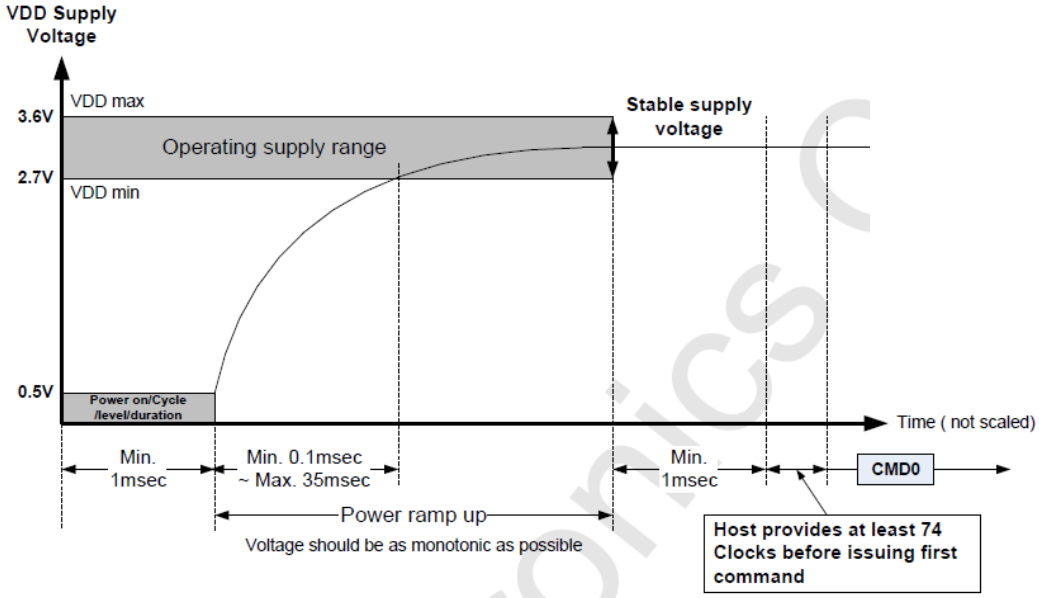
6.3 BUS Operating Conditions – Signal Line's Load

Total bus cpapcitance = CHOST + CBUS + N CCARD

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Capacitance of the card for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Caoacity Connected to Power Line	C_C		5	uF	To prevent inrush current

6.4 Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.
(1) Voltage level shall be below 0.5V
(2) Duration shall be at least 1ms.

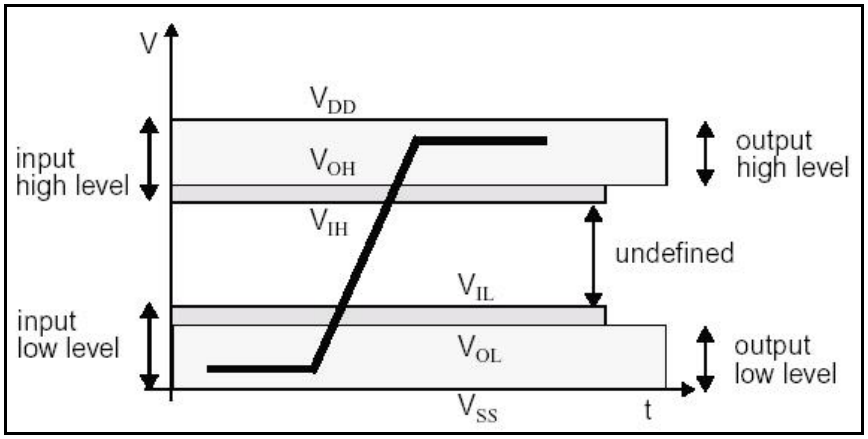
Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.
Followings are recommendations of Power ramp up:
(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
(4) Host shall wait until VDD is stable.
(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

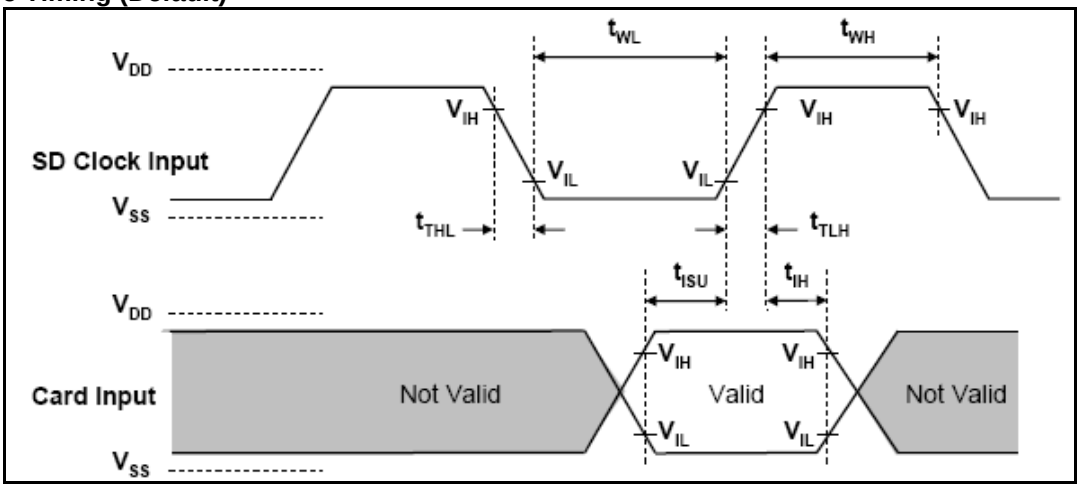
Power Down and Power Cycle

(1) When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
(2) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

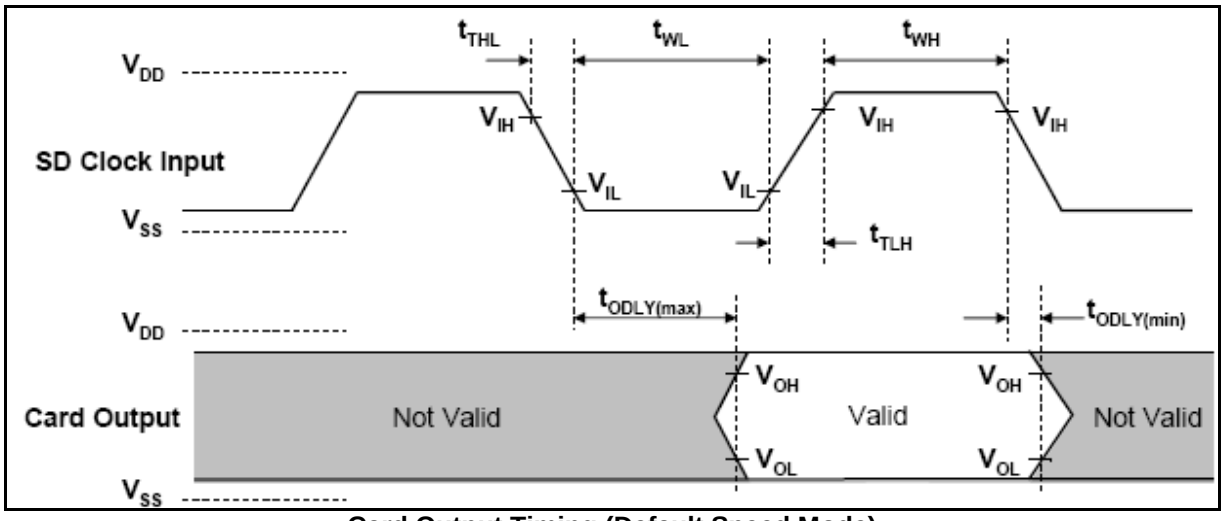
7. AC Characters



SD Interface Timing (Default)



Card Input Timing (Default Speed Card)

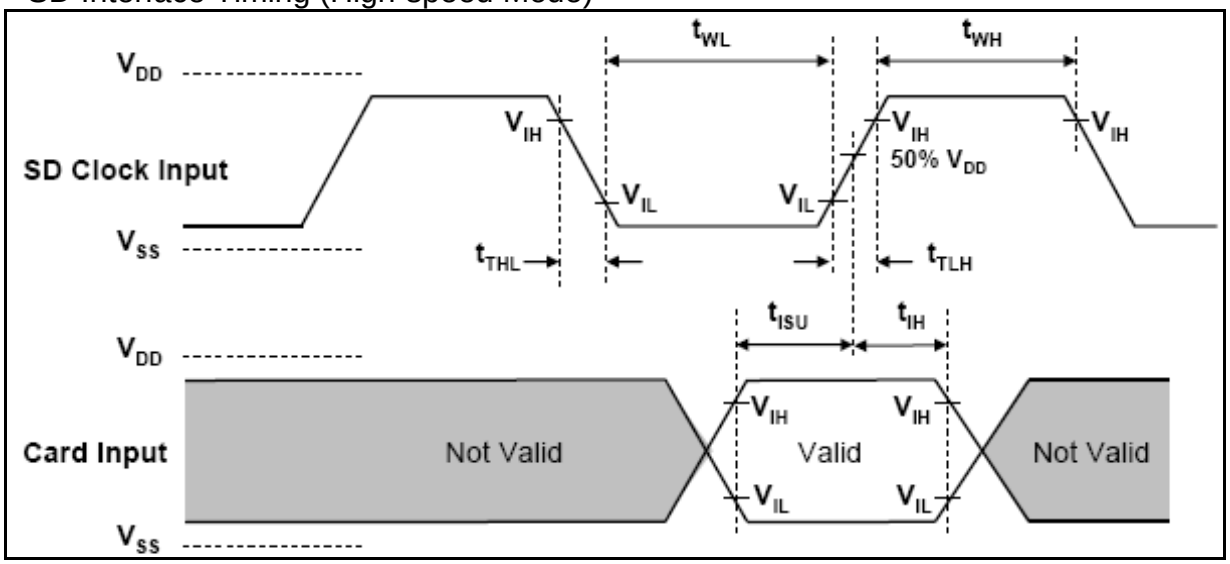


Card Output Timing (Default Speed Mode)

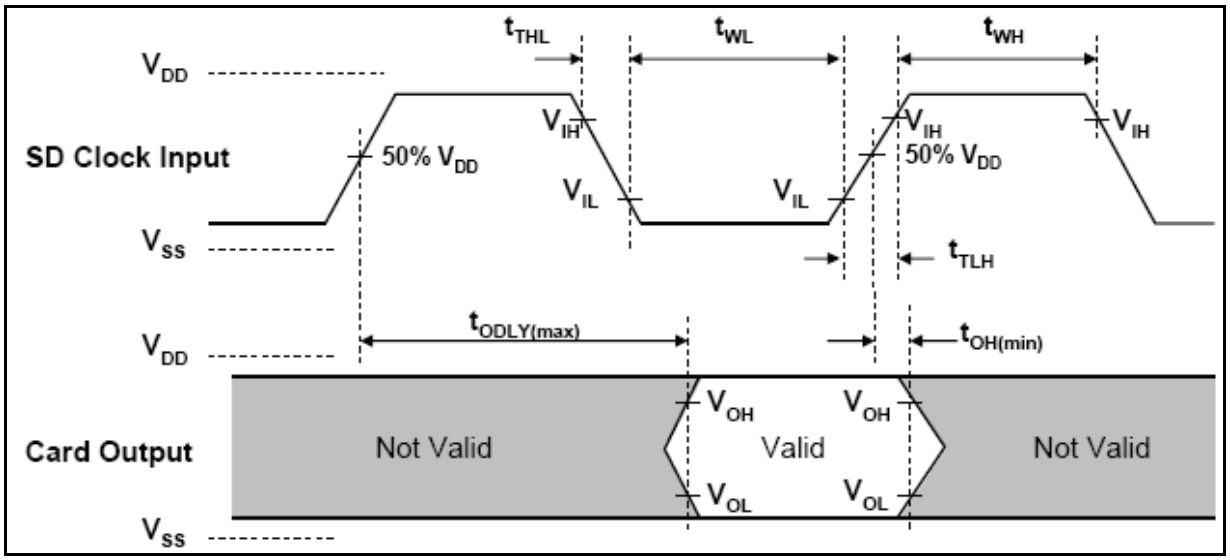
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L≤40 pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L≤40 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	C_L≤15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

7.1 SD Interface Timing (High-speed Mode)



Card Input Timing (High Speed Card)



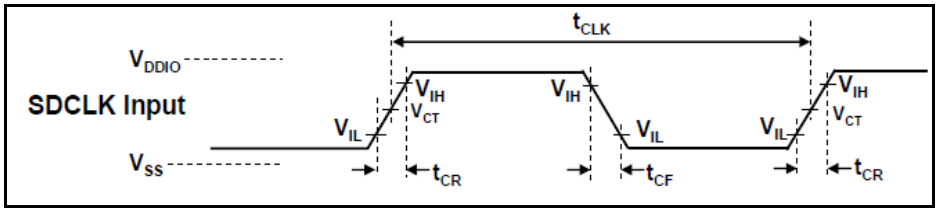
Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L≤40 pF (1 card)
Output Hold time	T_{OH}	2.5	50	ns	C_L≤15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL≤15 pF (1 card)

(1) In order to satisfy severe timing, host shall drive only one card.

7.2 SD Interface timing (SDR12, SDR25 and SDR50 and SDR104 Modes)

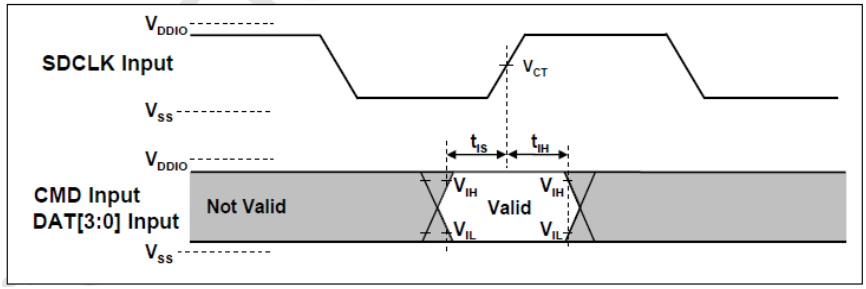
Input:



Symbol	Min	Max	Unit	Remark
tCLK	4.80	0	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2 * t_{CLK}	ns	tCR, tCF < 0.96ns (max.) at 208MHz, CCARD=10pF tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF The maximum value of tCR, tCF is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

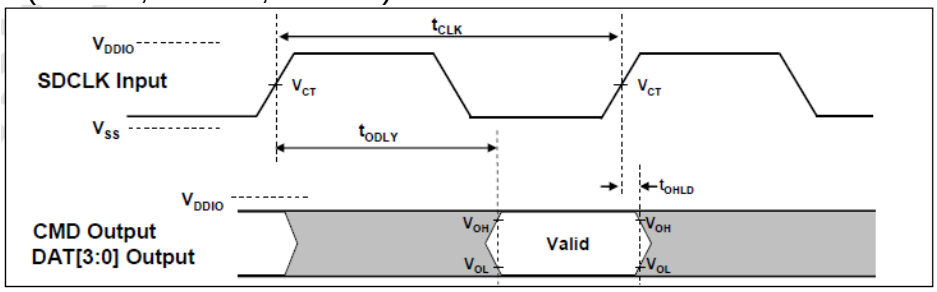
SDR50 & SDR104 Input Timing:



Symbol	Min	Max	Unit	SDR104 Mode
tIs	1.40	-	ns	C_{CARD} =10pF, VCT= 0.975V
tIH	0.80	-	ns	C_{CARD} =5pF, VCT= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
tIs	3.00	-	ns	C_{CARD} =10pF, VCT= 0.975V
tIH	0.80	-	ns	C_{CARD} =5pF, VCT= 0.975V

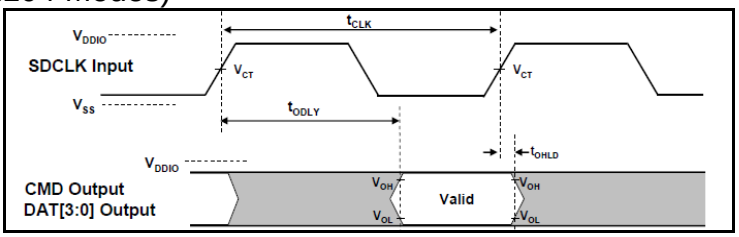
Card Input Timing

Output (SDR12, SDR25, SDR50)



Output Timing of Fixed Data Window

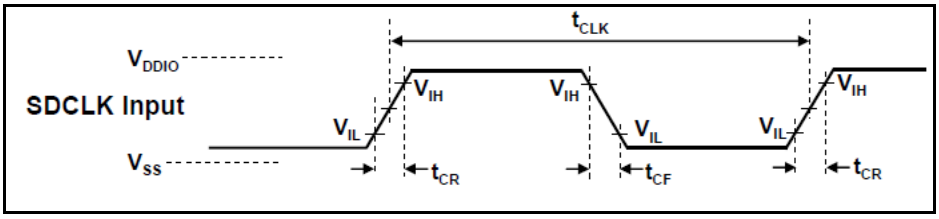
Output (SDR104 Modes)



Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

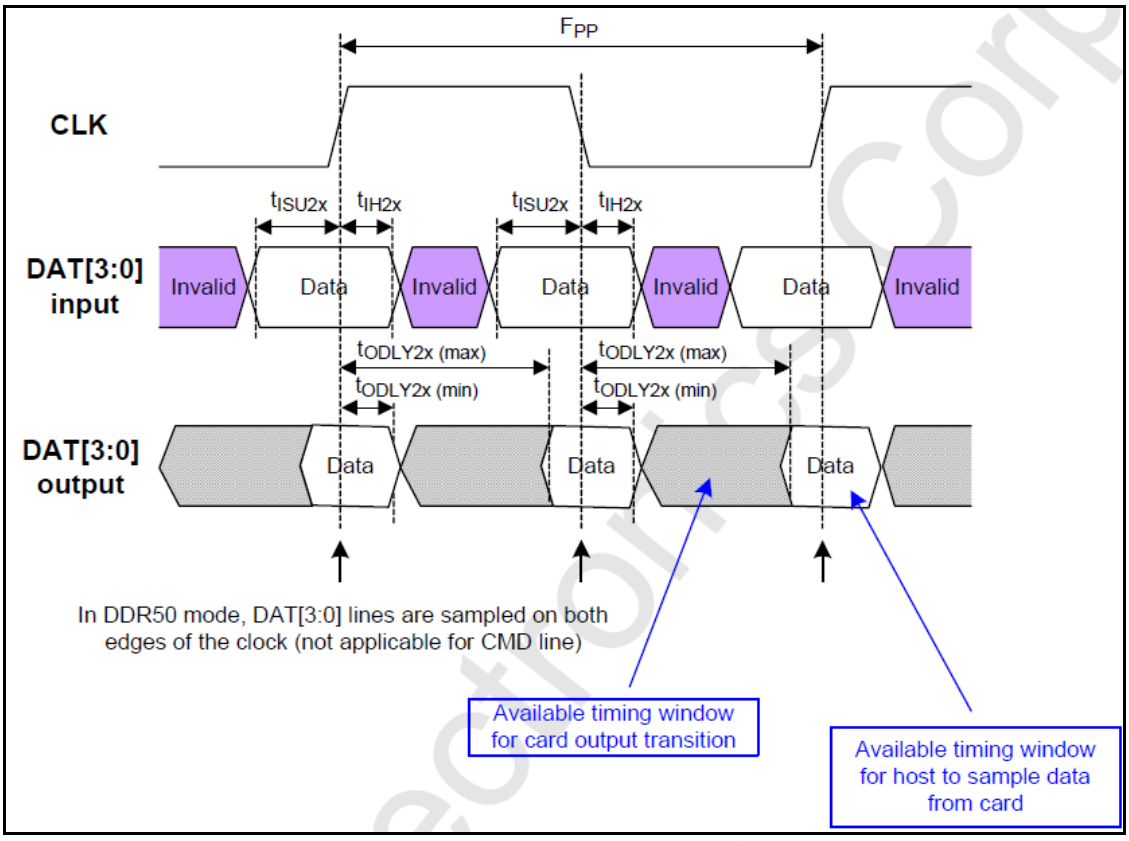
Output Timing of Fixed Data Window

7.3 SD Interface timing (DDR50 Modes)



Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2 * tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

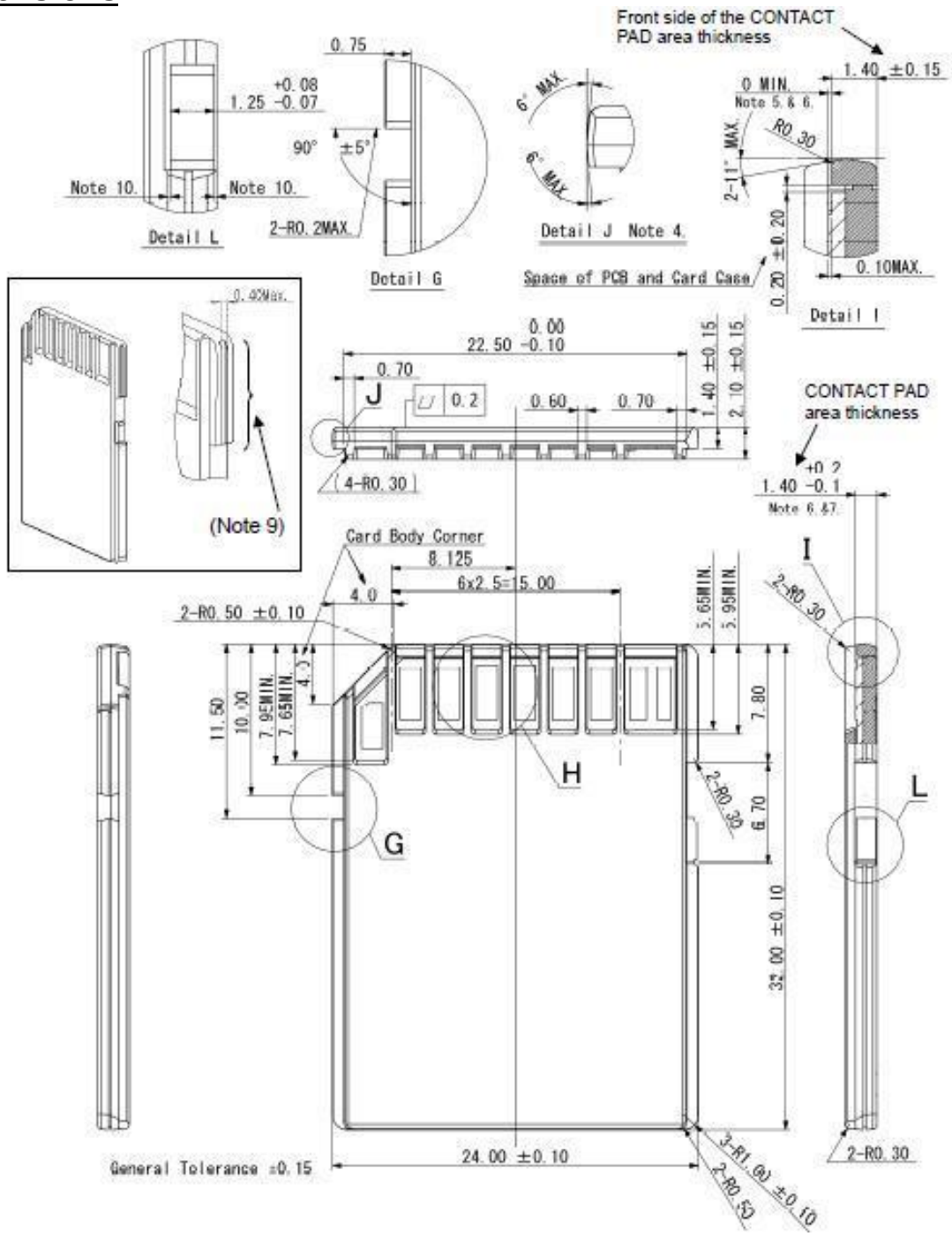
Clock Signal Timing



Timing Diagram DAT Inputs / Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_{card}≤ 30 pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_{card}≤ 10 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2X}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2X}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2X}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	t_{OH2X}	1.5	-	ns	C_L≥15 pF (1 card)

8. Dimensions



Dimensions of A SD Card (Bottom View, DIN)

Appendix: Part Number Table

3D TLC

Product	Advantech PN
SQF I-SD UHS-I 3D TLC (BiCS3) 16GB (0~70°C)	SQF-ISDV1-16G-D1C
SQF I-SD UHS-I 3D TLC (BiCS3) 32GB (0~70°C)	SQF-ISDV1-32G-D1C
SQF I-SD UHS-I 3D TLC (BiCS3) 64GB (0~70°C)	SQF-ISDV1-64G-D1C
SQF I-SD UHS-I 3D TLC (BiCS3) 128GB (0~70°C)	SQF-ISDV1-128G-D1C
SQF I-SD UHS-I 3D TLC (BiCS3) 256GB (0~70°C)	SQF-ISDV1-256G-D1C
SQF I-SD UHS-I 3D TLC (BiCS3) 16GB (-40~85°C)	SQF-ISDV1-16G-D1E
SQF I-SD UHS-I 3D TLC (BiCS3) 32GB (-40~85°C)	SQF-ISDV1-32G-D1E
SQF I-SD UHS-I 3D TLC (BiCS3) 64GB (-40~85°C)	SQF-ISDV1-64G-D1E
SQF I-SD UHS-I 3D TLC (BiCS3) 128GB (-40~85°C)	SQF-ISDV1-128G-D1E
SQF I-SD UHS-I 3D TLC (BiCS3) 256GB (-40~85°C)	SQF-ISDV1-256G-D1E