SQFlash Micro SD Card A1 C10 Datasheet

(SQF-MSDV1-xG-D1x)

CONTENTS

Revision History

Rev.	Date	History
0.1	2019/12/20	1. 1st draft

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1. Overview

The SQFlash Micro Secure Digital card (SQF-MSD) is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.00 Final] Specifications.

The microSD 6.10 card comes with 8-pin interface, designed to operate at a maximum operating frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. Its capacity could reach 256GB with exFAT SDXC.

SQFlash Industrial micro Secure Digital 6.10 card is one of the most popular cards today based on its high performance, good reliability and wide compatibility. Not to mention that it's well adapted for hand-held applications in semi-industrial/medical markets already.

2. Standard Features

- **Support File System Specification version 3.0**
- **Card capacity of non-secure area and secure area support [Part 3 Security Specification Ver4.0 Final] Specifications**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards**
- **Bus Speed Mode (using 4 parallel data lines)**
  - UHS-I mode
    - SDR12 - SDR up to 25MHz 1.8V signaling
    - SDR25 - SDR up to 50MHz 1.8V signaling
    - SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
    - SDR104: 1.8V signaling, Frequency up to 208MHz, up to 104MB/sec
    - DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec

  Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- **The command list supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions**
- **Copyrights Protection Mechanism**
  - Compliant with the highest security of SDMI standard
- **Support CPRM (Content Protection for Recordable Media) of SD Card**
- **Password Protection of cards (optional)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **+4KV/-4KV ESD protection in contact pads**
- **Operation voltage range: 2.7 ~ 3.6V**

3. Additional Features

■ Capacities

– 3D TLC type：32GB，64GB，128GB，256GB

■ Performance

Capacity	Specification	TestMetrixTest @500MB	
		Read (MB/s)	Write (MB/s)
32GB	A1, V10, C10, high reliability	95	20
64GB	A1, V30, C10, high reliability	95	25
128GB	A1, V30, C10, high reliability	95	30
256GB	A1, V30, C10, high reliability	95	30

■ Temperature Ranges

– Commercial Temperature
  - 0℃ to 70℃ for operating
  - -40℃ to 85℃ for storage

– Industrial Temperature
  - -40℃ to 85℃ for operating
  - -40℃ to 85℃ for storage

■ Mechanical Specification

– Shock：1,500G, Peak / 0.5ms
– Vibration：20G, Peak / 20~2000Hz
– Drop: 1.5m free fall
– Bending: ≥ 10N, hold 1min / 5times
– Torque: 0.15N-m or +/-2.5deg
– Salt Spray:
  - Concentration: 3% NaCl
  - Temperature: 35℃
  - Storage for 24 HRS
– Waterproof: JIS IPX7 compliance

■ Humidity

– Operating Humidity：5% ~ 93%
– Non-Operating Humidity：5% ~ 93%

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a flash drive can be written which is a measurement of flash drive's expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (Flash Drive Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 60,000 cycles
  - Ultra MLC: 20,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC: 3,000 cycles
- **Flash Drive Capacit**y: Physical capacity in total of a Flash Drive.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a flash drive controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

The TBW rating for a flash drive shall be derived for and verified under the following workload conditions,

- Sequential Write (copy file into card)
- P/E cycles incurred: erase count after writing – erase count before writing

4. Flash Management

Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQF-MSD applies the SECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption.

Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

SQF-MSD provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

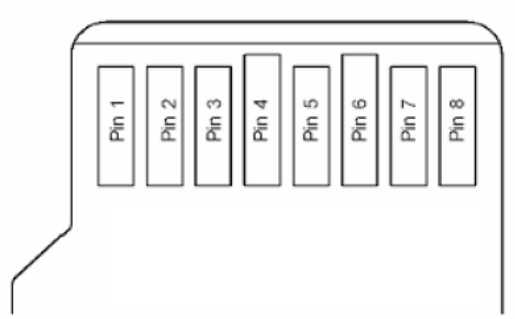
Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. MicroSD implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

Auto-Read Refresh

Auto-Read Refresh is especially applied on devices that read data mostly but rarely write data, such as GPS. When blocks are continuously read, then the device cannot activate wear leveling since it can only be applied while writing data. Thus, errors will accumulate and become uncorrectable. Accordingly, to avoid errors exceed the amount ECC can correct and blocks turn bad, It’s firmware will automatically refresh the bit errors when the error number in one block approaches the threshold, ex., 24 bits.

5. Pin Assignment and Block Diagram



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

(1) S: power supply, I: input; O: output using push-pull drivers; PP:I/O using push-pull driver
(2) The extended DAT lines (DAT1-DAT3)are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.
(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

6. Power Consumption

Table list as below is the power consumption of SQF-MSD card with different type of flash memory.

Capacity	Flash Structure	Read (mA)	Write (mA)	Idle (mA)
32GB	32GB x 1	400	400	1
64GB	32GB x 2	400	400	1
128GB	32GB x 4	400	400	1
256GB	32GB x 8	400	400	1

(1) Data transfer mode is single channel.

7. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	Ta	Operating Temperature	-40	+85	℃
2	Tst	Storage Temperature	-40	+85	℃

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	-40	+85	℃
V_{DD} Voltage	V_{DD}	2.7	3.6	V

8. DC Characters

8.1 Bus Operation Conditions for 3.3V Signaling

Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

8.2 Bus Signal Line Levels

Bus Operation Conditions – Signal Line's Load

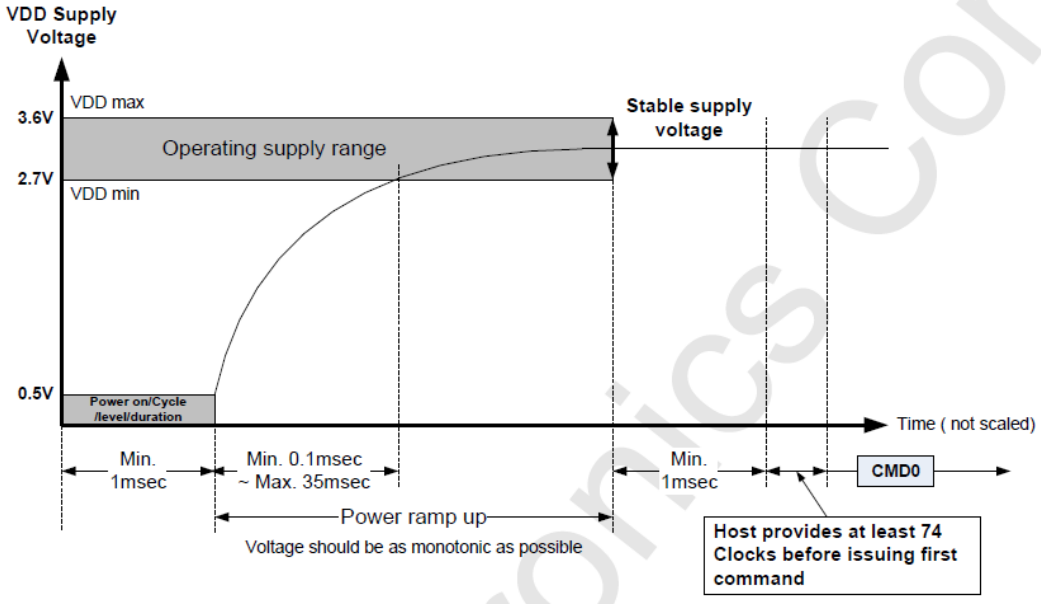
Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10[1]	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

<Note 1> PS8131 is SD and eMMC(4.51) controller, so the maximum of eMMC capacitance will be 12pF.

8.3 Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

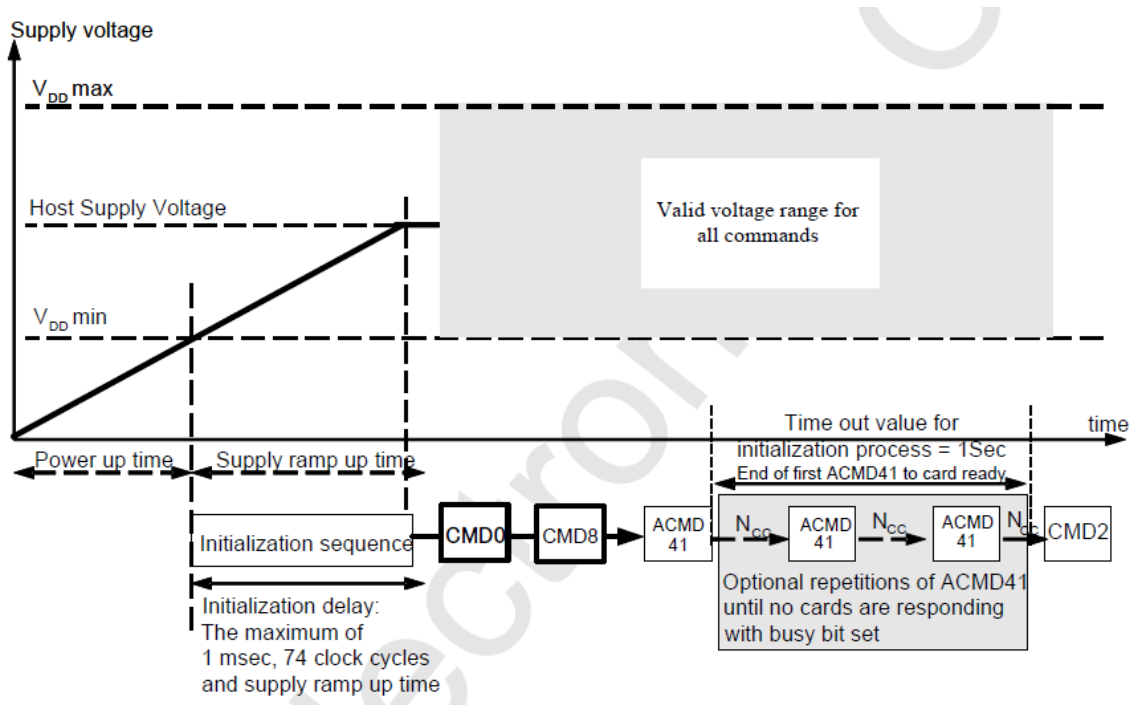
Power Down and Power Cycle

• When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

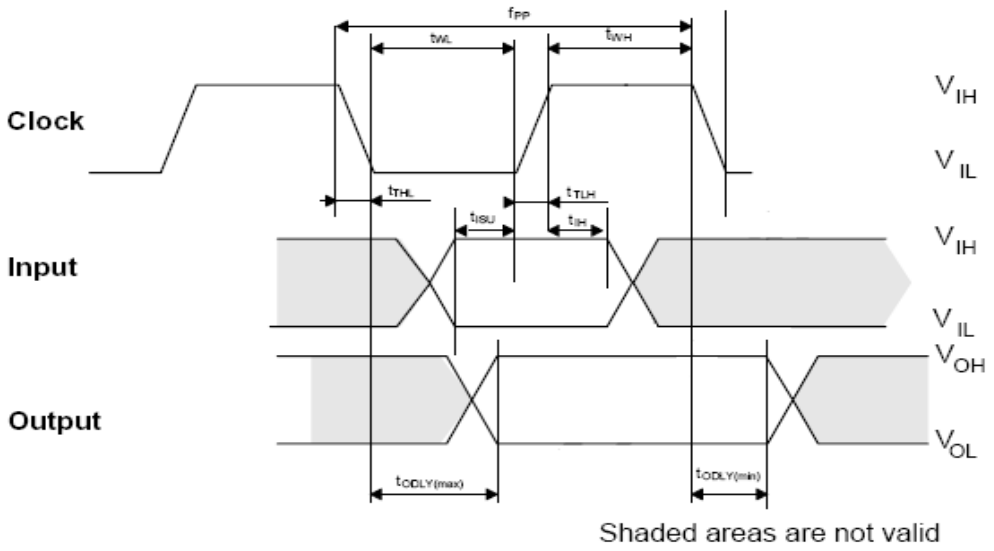
8.4 Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.



8.5 AC Characteristic

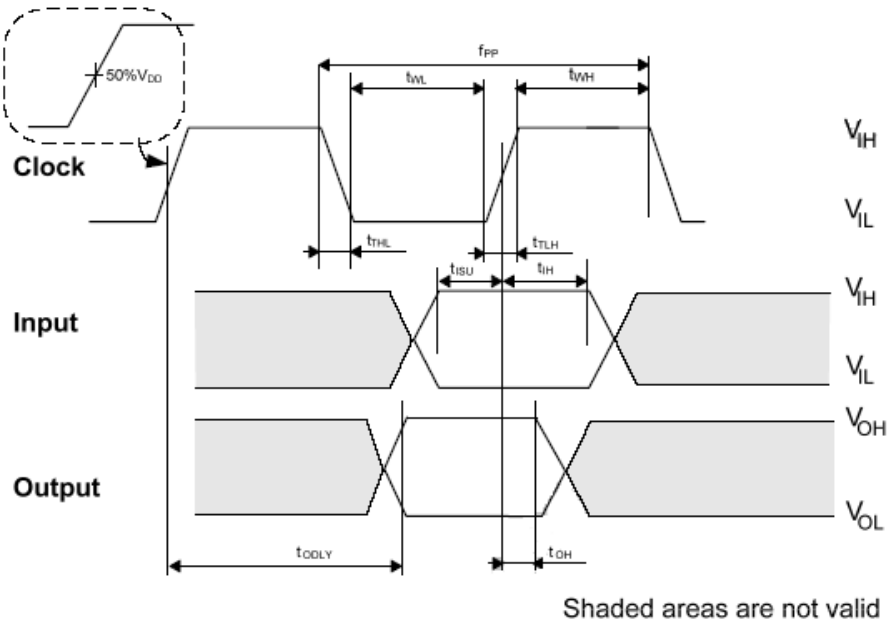
8.5.1 microSD Interface timing (Default)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	kHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

8.5.2 microSD Interface Timing (High-Speed Mode)

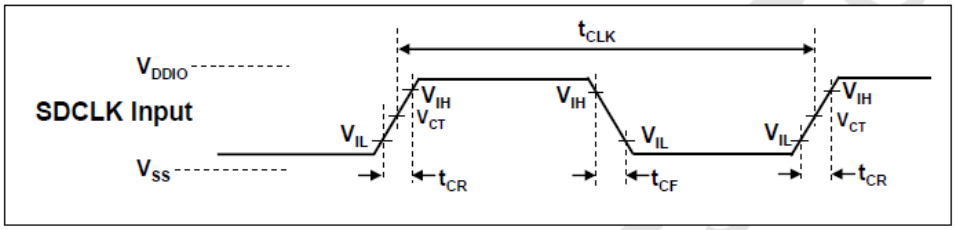


Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{card} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{card} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40$ pF (1 card)
Output Hold time	T_{OH}	2.5		ns	$C_L \leq 15$ pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

8.5.3 microSD Interface timing (SDR12, SDR25, SDR50 and SDR 104 Modes)

Input:

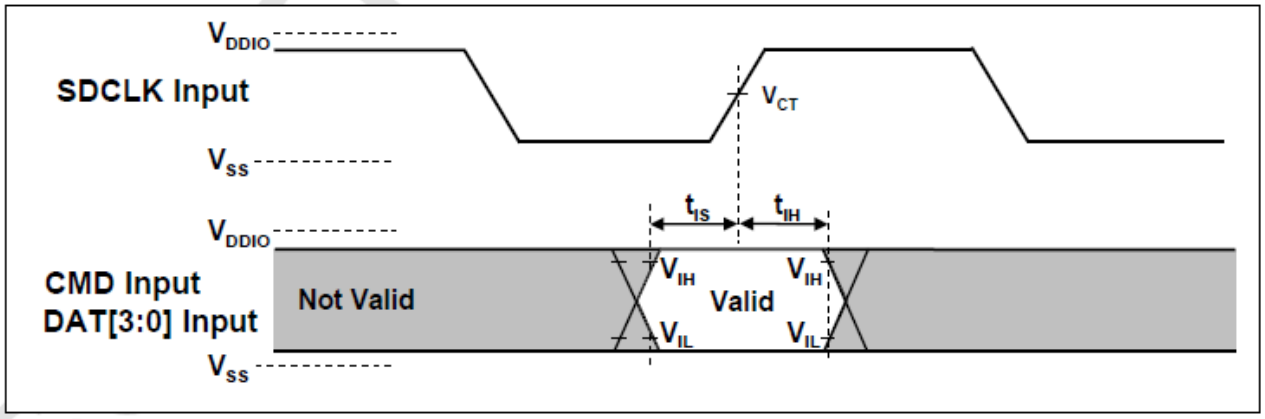


Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Clock Signal Timing

SDR50 and SDR104 Input Timing:

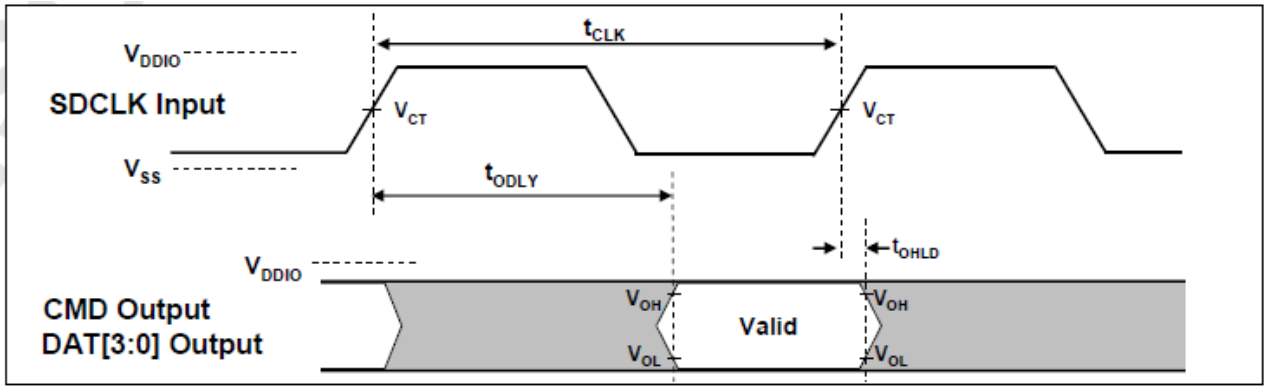


Card Input Timing

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8[1]	-	ns	C_{CARD} = 5pF, V_{CT}= 0.975V

<Note 1> PS8131 is SD and eMMC(4.51) controller, so the maximum C_{CARD} becomes 12pF and minimum of t_{IH} will be 1.10 ns.

Output:

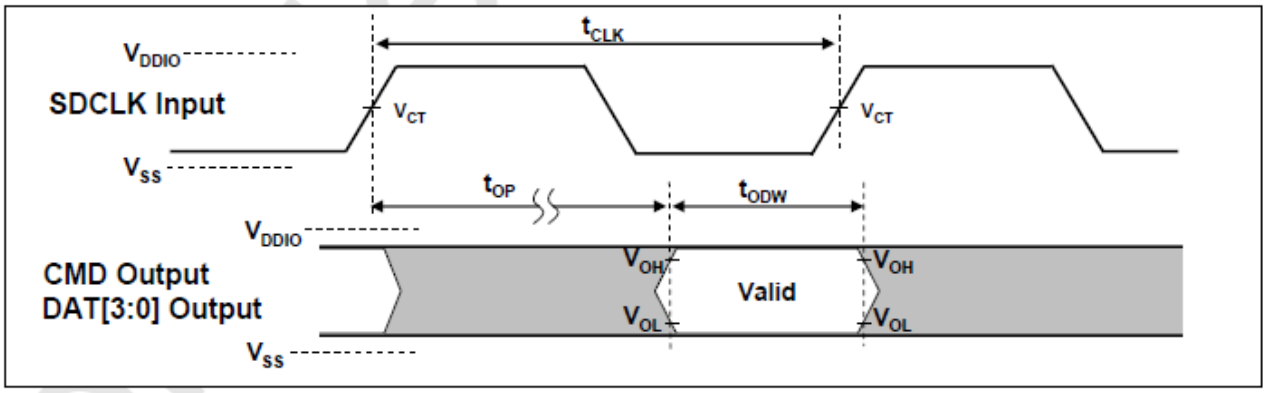


Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

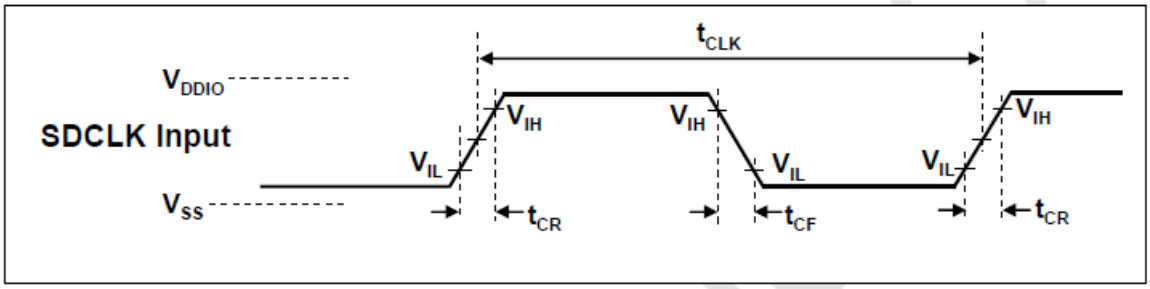
Output Timing of Fixed Data Window

Output (SDR104 mode):



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

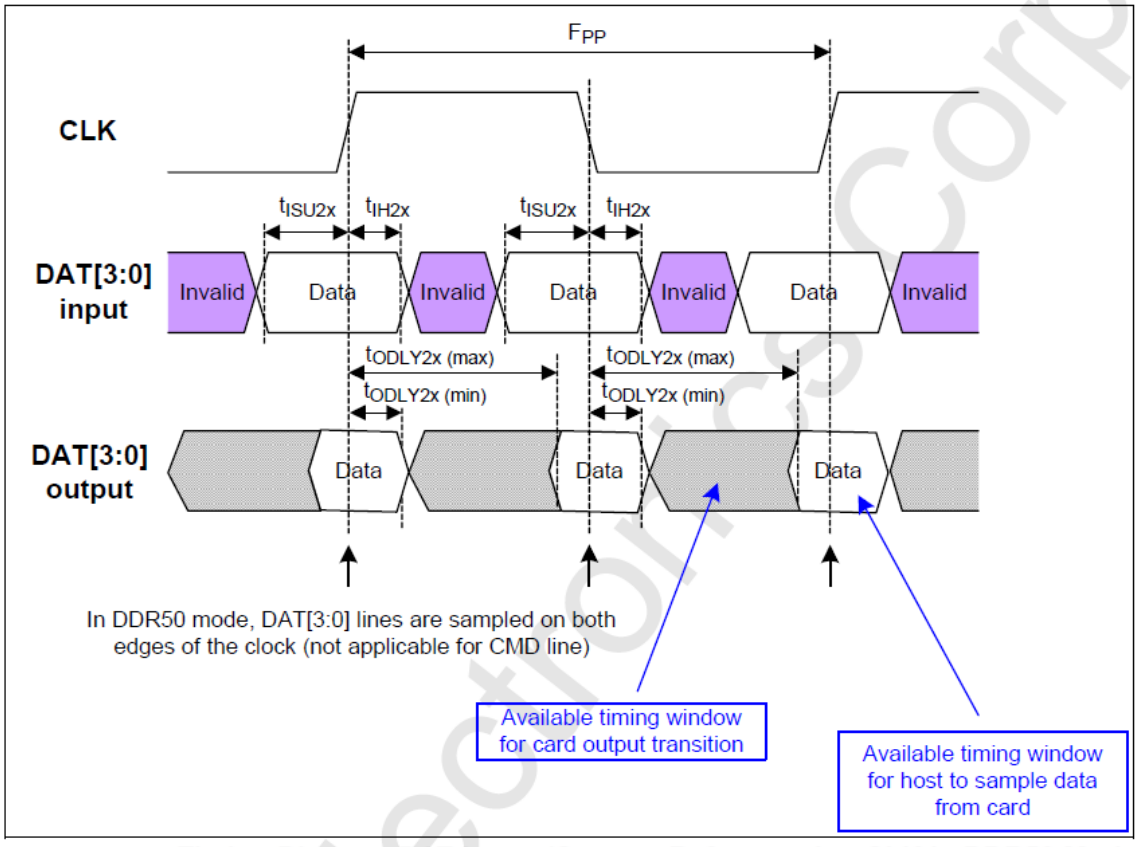
8.5.4 microSD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Clock Signal Timing

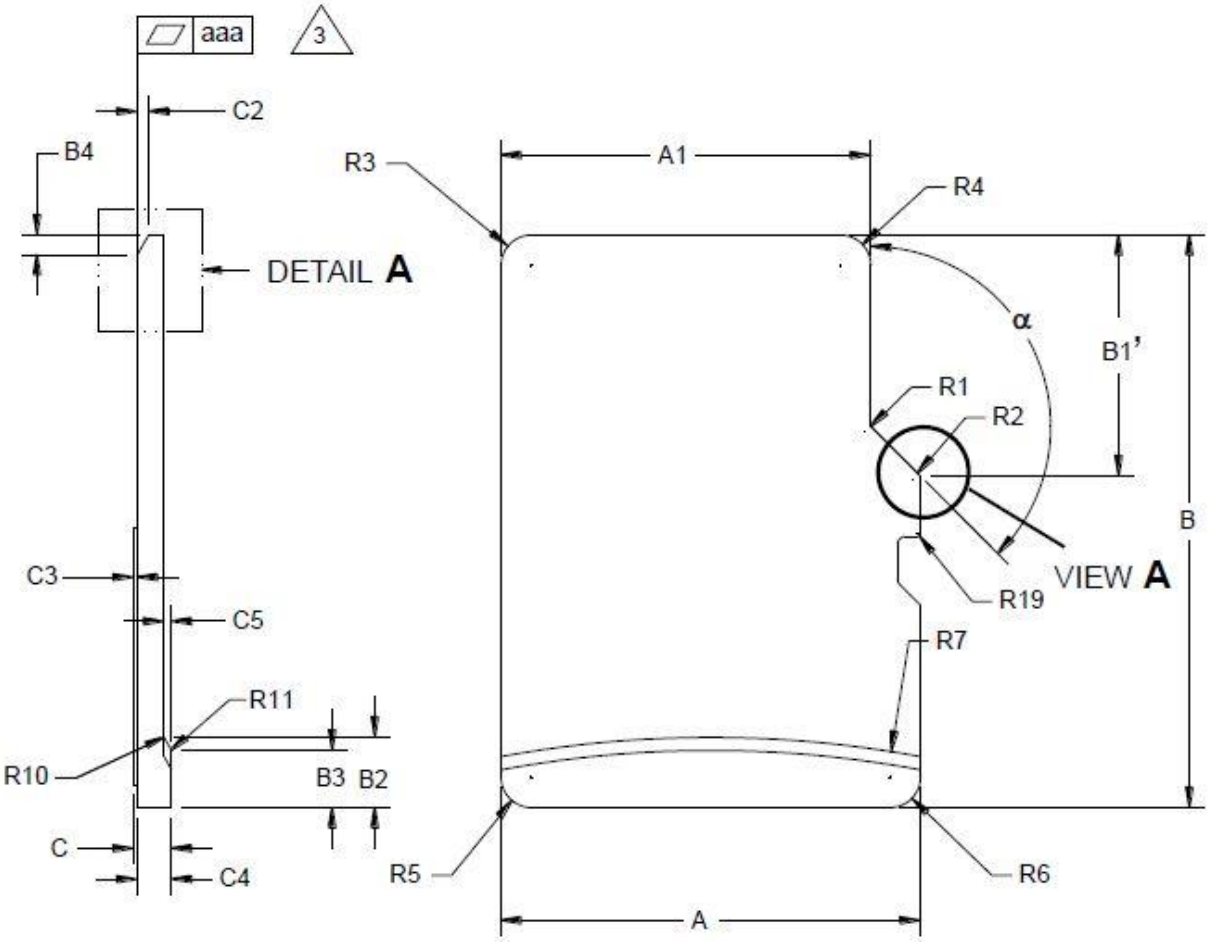


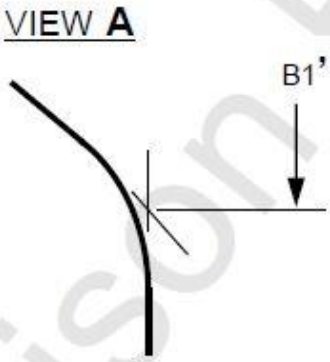
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

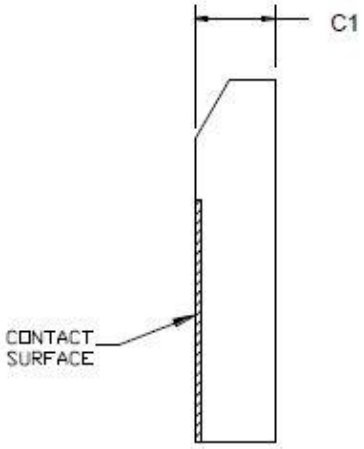
Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_L≤30 pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

Bus Timings – Parameters Values (DDR50 mode)

9. Dimensions

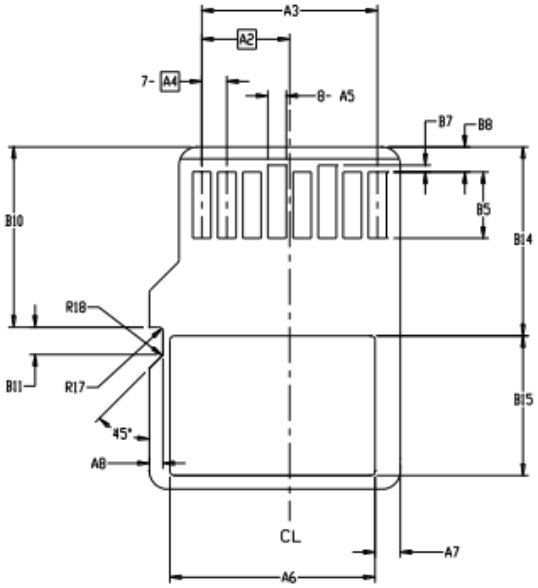






DETAIL A

As measurement point is changed like as VIEW A, symbol B1 is changed to symbol B1'. There is no modification in mechanical dimension.



Type A

	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
A14	0.05	-	-	
A15	5.71	5.81	5.91	
A16	6.47	6.57	6.67	
A17	6.62	6.72	6.82	
A18	7.38	7.48	7.58	
A19	7.75	7.85	7.95	
A20	8.55	8.65	8.75	
A21	0.90	-	-	
A22	-	-	8.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
B16	5.80	5.90	6.00	
B17	0.20	0.30	0.40	
B18	7.80	8.80	8.90	
B19	8.70	8.80	8.90	
B20	-	3.20	-	REF
B21	1.90	2.00	2.10	
B22	9.00	-	-	
B23	0.10	-	-	

Notes:

1. DIMENSIONING and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. COPLANARITY is additive to C1 MAX thickness.
4. All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment."
5. Refer to Appendix E about test method of warpage.
6. As measurement point is changed, symbol B1 is changed to symbol B1'.
7. C4 and C5 are added from Version 4.00.

Appendix: Part Number Table

Product	Advantech PN
SQF SDXC A1 C10 3D TLC 32G, 1CH (0~70°C)	SQF-ISDV1-32G-D1C
SQF SDXC A1 C10 3D TLC 64G, 1CH (0~70°C)	SQF-ISDV1-64G-D1C
SQF SDXC A1 C10 3D TLC 128G, 1CH (0~70°C)	SQF-ISDV1-128G-D1C
SQF SDXC A1 C10 3D TLC 256G, 1CH (0~70°C)	SQF-ISDV1-256G-D1C
SQF SDXC A1 C10 3D TLC 32G, 1CH (-40~85°C)	SQF-ISDV1-32G-D1E
SQF SDXC A1 C10 3D TLC 64G, 1CH (-40~85°C)	SQF-ISDV1-64G-D1E
SQF SDXC A1 C10 3D TLC 128G, 1CH (-40~85°C)	SQF-ISDV1-128G-D1E
SQF SDXC A1 C10 3D TLC 256G, 1CH (-40~85°C)	SQF-ISDV1-256G-D1E