SODIMM DDR3L 1600 8GB Datasheet

(SQR-SD3I-8G1K6SNLB)

CONTENTS

Revision History

Rev	Date	Modification
1.0	13th Apr. 2016	Official released.
2.0	26th Mar., 2017	Modified EEPROM dimension

1. Description

The SQR-SD3I-8G1K6SNLB is a 1024MB x 64bits DDR3L-1600 2 Rank SO-DIMM. It consists of 16pcs 512Mx8bits DDR3L SDRAMs FBGA packages and a 2048 bits serial EEPROM on a 204-pin printed circuit board. The SQR-SD3I-8G1K6SNLB is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. Features

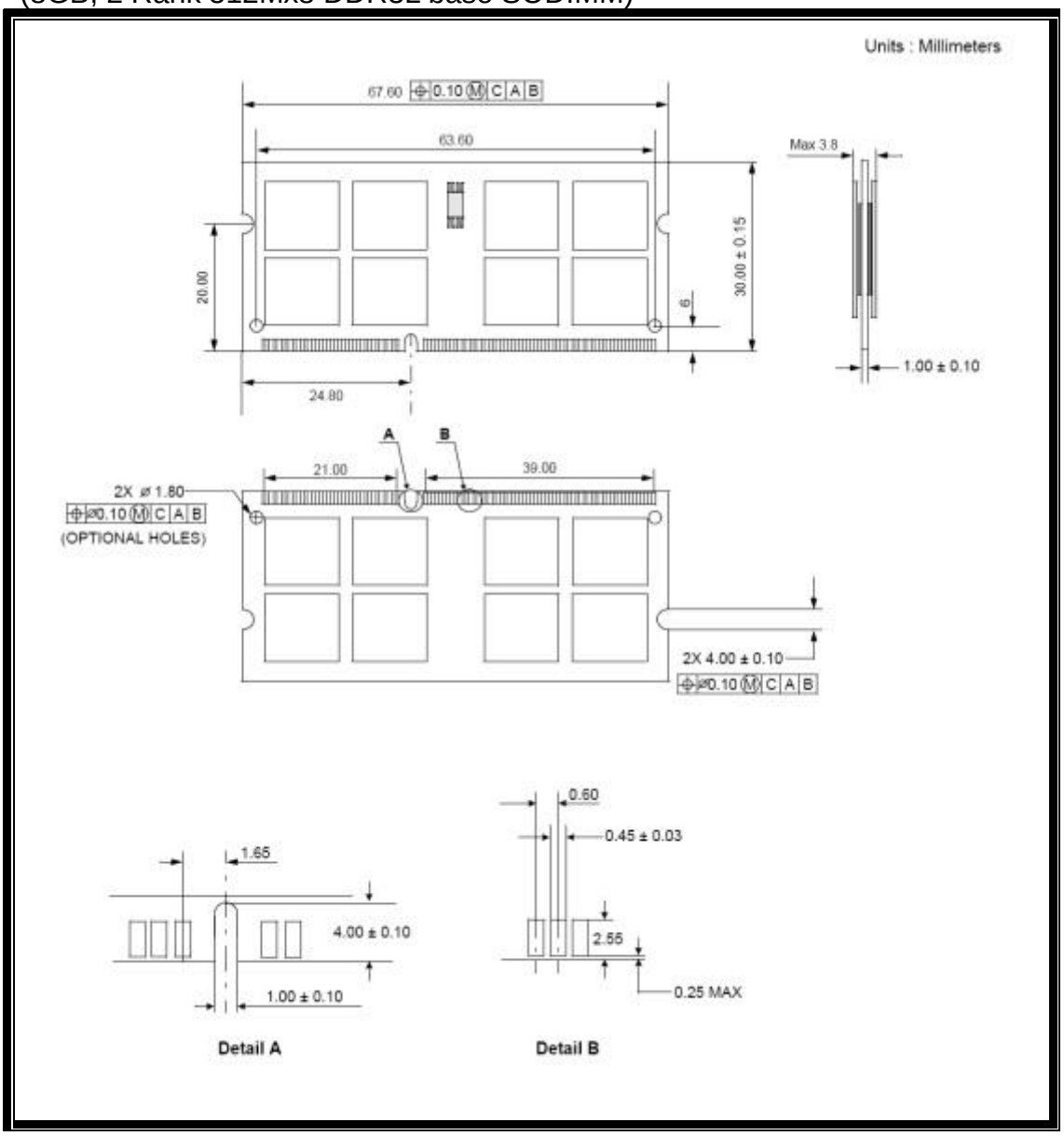
- Key Parameter

Industry Nomenclature	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
	CL=7	CL=9	CL=11			
PC3-12800	1066	1333	1600	13.125	13.125	13.125

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- Cl-tRCD-tRP: 11-11-11
- VDD=VDDQ= 1.35 Volt (-0.067V/+0.1V) or 1.5Volt (-0.1V/+0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- On-Board thermal sensor (Class B)
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (TA ≤ +85°C)
- 15/10/1 Addressing (row/column/rank)-8GB
- Golden Connector (Au: 30μ")
- SDRAM operating temperature range -40°C ≤ T_{CASE} ≤ +85°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7, 9, 11
  - Burst Length: switch on-the-fly: BL=8 or BC 4

3. Dimension

(8GB, 2 Rank 512Mx8 DDR3L base SODIMM)



Note: Device position is only for reference.

4. Pin Identification

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	VDD	Power Supply
/WE	SDRAM write enable	VDDID	VDD Identification Flag
/S0 - /S1	DIMM Rank Select Lines	VDDQ	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	VREFDQ	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	VREFCA	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	VSS	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	VDDSPD	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	VTT	SDRAM I/O termination supply.

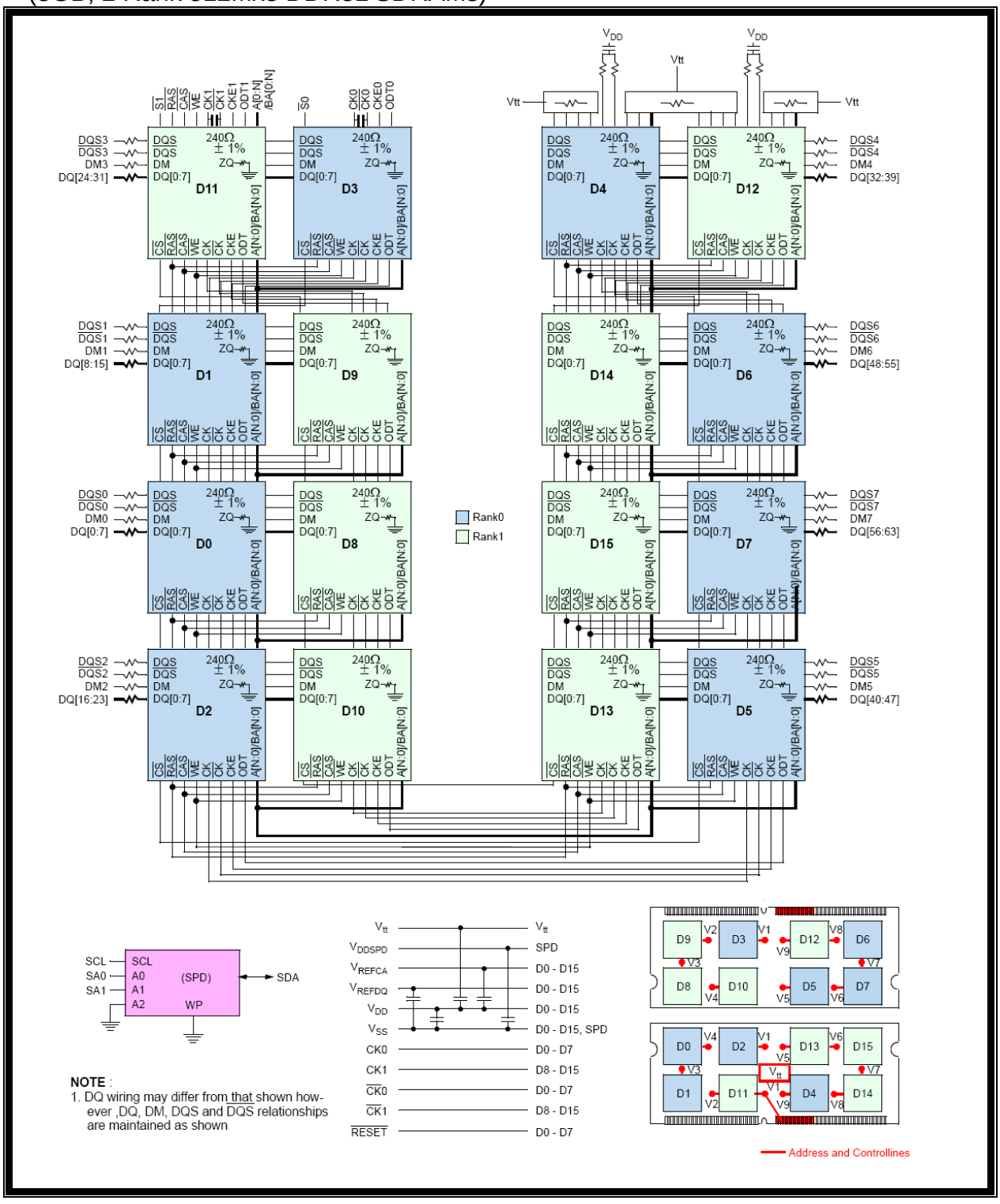
5. Pin Configurations

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	2	V_{SS}	69	DQ27	70	DQ31	137	DQS4	138	V_{SS}
3	V_{SS}	4	DQ4	71	V_{SS}	72	V_{SS}	139	V_{SS}	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1	141	DQ34	142	DQ39
7	DQ1	8	V_{SS}	75	V_{DD}	76	V_{DD}	143	DQ35	144	V_{SS}
9	V_{SS}	10	/DQS0	77	NC	78	A15 ***	145	V_{SS}	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14 ***	147	DQ40	148	DQ45
13	V_{SS}	14	V_{SS}	81	V_{DD}	82	V_{DD}	149	DQ41	150	V_{SS}
15	DQ2	16	DQ6	83	A12, /BC	84	A11	151	V_{SS}	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	V_{SS}	20	V_{SS}	87	V_{DD}	88	V_{DD}	155	V_{SS}	156	V_{SS}
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	V_{SS}	26	V_{SS}	93	V_{DD}	94	V_{DD}	161	V_{SS}	162	V_{SS}
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/Reset	97	A1	98	A0	165	DQ49	166	DQ53
31	V_{SS}	32	V_{SS}	99	V_{DD}	100	V_{DD}	167	V_{SS}	168	V_{SS}
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	V_{SS}
37	V_{SS}	38	V_{SS}	105	V_{DD}	106	V_{DD}	173	V_{SS}	174	DQ54
39	DQ16	40	DQ20	107	A10, /AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	V_{SS}
43	V_{SS}	44	V_{SS}	111	V_{DD}	112	V_{DD}	179	V_{SS}	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/S0	181	DQ56	182	DQ61
47	DQS2	48	V_{SS}	115	/CAS	116	ODT0	183	DQ57	184	V_{SS}
49	V_{SS}	50	DQ22	117	V_{DD}	118	V_{DD}	185	V_{SS}	186	/DQS7
51	DQ18	52	DQ23	119	A13 ***	120	ODT1	187	DM7	188	DQS7
53	DQ19	54	V_{SS}	121	/S1	122	NC *	189	V_{SS}	190	V_{SS}
55	V_{SS}	56	DQ28	123	V_{DD}	124	V_{DD}	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST/NC	126	V_{REFCA}	193	DQ59	194	DQ63
59	DQ25	60	V_{SS}	127	V_{SS}	128	V_{SS}	195	V_{SS}	196	V_{SS}
61	V_{SS}	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDD_{SPD}	200	SDA
65	V_{SS}	66	V_{SS}	133	V_{SS}	134	V_{SS}	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	Vtt	204	Vtt

* NC = No Connect
** TEST (PIN# 125) reserve for bus probing, is NC on normal modules.
*** Pin might conneceted to NC ball od DRAMs (depanding on density); alternatively may connect to termination resistor

6. Block Diagram

(8GB, 2 Rank 512Mx8 DDR3L SDRAMs)



Note: Temperature sensor accuracy (max):

- ± 1 °C from +75 °C to +95 °C
- ± 2 °C from +40 °C to +125 °C
- ± 3 °C from –40 °C to +125 °C

7. Parameter & Operating Conditions

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating Temperature	TCASE	-40 to +85	°C	1,2

Note: 1. Operating Temperature Tcase is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. At -40 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on VDD relative to Vss	VDD	-0.4 to +1.975	V	1,3
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4 to +1.975	V	1,3
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 to +1.975	V	1
Storage temperature	TSTG	-50 to 150	°C	1,2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.5)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.283	1.35	1.45	V	1,2
Supply voltage for Output	VDDQ	1.283	1.35	1.45	V	1,2
I/O Reference voltage (DQ/DM)	$VREF_{DQ}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3,4
I/O Reference voltage (CMD/ADD)	$VREF_{CA}$(DC)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3,4
AC Input logic high	VIH(AC)	VREF+0.175	-	-	V	5
AC Input logic low	VIL(AC)	-	-	VREF-0.175	V	5
DC Input logic high	VIH(DC)	VREF+0.1	-	VDD	V	5
DC Input logic low	VIL(DC)	VSS	-	VREF-0.1	V	5

Note: There is no specific device VDD supply voltage requirement for SSTL-1.5 compliance.
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD (for reference: approx. VDD/2 +/-15mV)
4. For DQ and DM, VREF=VREFDQ. For input only pins except RESET, or VREF=VREFCA.
5. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.

AC Input Level for Differential Signals

Parameter	Symbol	Value		Unit	Notes
Differential Input Logical High	VIHdiff	+0.2	-	V	1
Differential Input Logical Low	VILdiff	-	-0.2	V	1

Note: 1.Used to define a differential signal slew-rate

Operating, Standby, and Refresh Currents

- 8GB SODIMM (2 Rank, 512Mx8 DDR3L SDRAMs TCASE = -40 °C ~ 85 °C)

Parameter		Symbol	PC3-12800	Unit
One bank; Active - Precharge		I DD0	480	mA
One bank; Active - Read - Precharge		I DD1	550	mA
Precharge Standby Current		I DD2N	320	mA
Precharge Power Down Current		I DD2P	240	mA
Pecharge Quiet Standby Current		I DD2Q	320	mA
Active Standby Current		I DD3N	400	mA
Precharge Power Down Current	Fast Mode	I DD3P	320	mA
Precharge Power Down Current	Slow Mode	I DD3P	320	mA
Operating Current Burst Read		I DD4R	900	900
Operating Current Burst Write		I DD4W	1040	1040
Burst Refresh Current		I DD5B		1210
Self-Refresh Current: Normal Temperature Range		I DD6		240
Operating Bank Interleave Read Current		I DD7	1210	1380
Reset Low-Current		IDD8	240	240

Timing Parameters & Specifications

(T_{CASE} = -40 °C ~ 85 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Parameter	Symbol	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
Minimum Clock Cycle Time	tCK (DLL-Off)	8	-	ns
Average Clock Period	tCK (avg)	1.5	3.3	ns
Average high pulse width	tCH (avg)	0.47	0.53	tCK (avg)
Average low pulse width	tCL (avg)	0.47	0.53	tCK (avg)
Absolute Clock Period	tCK (abs)	tCK(avg)min +tJIT(per)min	tCK(avg)max+ tJIT(per)max	Ps
Absolute high pulse width	tCH (abs)	0.43	-	tCK (avg)
Absolute low pulse width	tCL (abs)	0.43	-	tCK (avg)
Clock Period Jitter	JIT (per)	-70	70	Ps
Clock Period Jitter during DLL locking period.	TJIT (per, lck)	-60	60	Ps
Cycle to Cycle Period Jitter	JIT (CC)	140		Ps
Cycle to Cycle Period Jitter during DLL locking period.	TJIT (CC, lck)	120		Ps
	TJIT (duty)	-	-	Ps
Cumulative error across 2 cycle	TERR (2per)	-103	103	Ps
Cumulative error across 3 cycle	TERR (3per)	-122	122	Ps
Cumulative error across 4 cycle	TERR (4per)	-136	136	Ps
Cumulative error across 5 cycle	TERR (5per)	-147	147	Ps
Cumulative error across 6 cycle	TERR (6per)	-155	155	Ps
Cumulative error across 7 cycle	TERR (7per)	-163	163	Ps
Cumulative error across 3 cycle	TERR (8per)	-169	169	Ps
Cumulative error across 4 cycle	TERR (9per)	-175	175	Ps
Cumulative error across 5 cycle	TERR (10per)	-180	180	Ps
Cumulative error across 6 cycle	TERR (11per)	-184	184	Ps
Cumulative error across 7 cycle	TERR (12per)	-188	188	Ps
Cumulative error across 13~50 cycle	TERR (nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) *		Ps

		tJIT(per)max		
Data Timing				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
DQS, DQS# to DQ skew, per group, per access	tDSQ	-	100	Ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ (DQ)	-450	225	Ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	225	Ps
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	10	-	Ps
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	45	-	Ps
Data Strobe Timing				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
DQS,DQS# differential READ Preamble	tRPRE	0.9		tCK(avg)
DQS, DQS# differential READ Postamble	tRPST	0.3		tCK(avg)
DQS, DQS# differential output high time	tQSH	0.4		tCK(avg)
DQS, DQS# differential output low time	tQSL	0.4		tCK(avg)
DQS, DQS# differential WRITE Preamble	tWPRE	0.9		tCK(avg)
DQS, DQS# differential WRITE Postamble	tWPST	0.3		tCK(avg)
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-225	225	Ps
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	Ps
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	Ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	tCK(avg)

DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	tCK(avg)
Command and Address Timing				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nC K, 7.5ns)	-	
Delay from start of internal write transaction to Internal read command	tWTR	max(4nC K, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max(12n CK, 15ns)	-	
Refer to Section 1 Feature	tRCD	Refer to Section 1 Feature		
Refer to Section 1 Feature	tRP	Refer to Section 1 Feature		
Refer to Section 1 Feature	tRC	Refer to Section 1 Feature		
	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL (min)	WR + roundup(tRP / tCK(avg))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1		nCK
ACTIVE to PRECHARGE command period	tRAS	35	9 tREFI	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 6ns)		
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 7.5ns)		
Four activate window for 1KB page size	tFAW	30		ns
Four activate window for 2KB page size	tFAW	40	-	ns
Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	tIS (base)	45		ns
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	170		ps
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	120		ps
Calibration Timing				

Parameter	Symbol	Min.	Max.	Unit
Power-up and RESET calibration time	tZQinit	Max. (512nCK, 640ns)	-	nCK
Normal operation Full calibration time	tZQoper	Max. (256nCK, 320ns)	-	nCK
Normal operation Short calibration time	tZQCS	Max. (64nCK, 80ns)	-	nCK
Reset Timing				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nC K,tRFC(min) +10ns)	-	
Self Refresh Timings				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Exit Self Refresh to commands not requiring a locked DLL	tXS	Max(5nCK), tRFC(min)+10ns)		
Exit Self Refresh to commands requiring a locked DLL.	tXSDLL	tDLL(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing.	tCKESR	tCKE9min)+1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max(5nCK,10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	Max(5nCK,10ns)	-	
Power Down Timings				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nC K, 6ns)	**-**	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCKCK, 24ns)	**-**	
CKE minimum pulse width	tCKE	max(3nCK,5ns)	**-**	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK

Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 +(tWR /tCK(avg)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 +WR + 1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 +(tWR /tCK(avg)	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	nCK
ODT Timings				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
RTT-turn-on	tAON	-225	225	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)

SERIAL PRESENCE DETECT SPECIFICATION

2RANK SODIMM DIMM based on 512Mx8, 8Banks, 8K Refresh, DDR3L SDRAMs with SPD

Byte	Description	Function Supported	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	112/256/176 Bytes	92	
1	SPD Revision	SPD Revision 1.1	11	
2	Key Byte/DRAM Device Type	DDR3-DRAM	0B	
3	Key Byte/Module type	SODIMM	03	
4	SDRAM Density and Banks	8 Banks, 4Gb	04	
5	SDRAM Address	15/11	21	
6	Reserve	1.35V Operable	02	
7	Module Organization	2 Rank x8	09	
8	Module Memory Bus Width	64bit Bus	03	
9	Fine Timebase (FTB) Dividend/Divisor	DDR3-Fine Timebase Dividend/Divisor	52	
10	Medium Timebase (MTB) Dividend	1ns	01	
11	Medium Timebase (MTB) Divisor	8	08	
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3-Min SDRAM Cycle Time	0A	
13	Reserve	Reserved	00	
14	CAS latency, least Significant Byte	DDR3-CAS LATENCIES SUPPORTED	FE	
15	CAS latency, most Significant Byte	DDR3-CAS LATENCIES SUPPORTED	00	
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69	
17	Minimum Write Recovery Time (tWRmin)	15ns	78	
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	DDR3-MIN ROW ACTIVE TO ROW ACTIVE DELAY	30	
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69	

21	Upper Nibbles for tRAS and tRC	Refer to Byte 22,23	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	35ns	18	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	48.75ns	81	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260ns	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260ns	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C	
28	Upper Nibble for tFAW	Refer Byte 29	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	DDR3-MIN FOUR ACTIVE WINDOW DELAY	F0	
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83	
31	SDRAM Thermal and Refresh Options	DDR3-SDRAM DEVICE THERMAL REFRESH OPTIONS	05	
32	Module Thermal Sensor	Thermal Sensor	00	
33	SDRAM Device Type	Mono-Die	00	
34-59	Reserve	Reserve	00	
60-63	Module Type Specific Section,	-	0F 11 05 00	
64-117	Reserve	-	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	-	06 F1	
119	Module ID: Module Manufacturing Location	-	02	
120-121	Module ID: Module Manufacturing Date	-	0A 03	
122-125	**Module Serial Number**	-	00	
126-127	**SPD Cyclical Redundancy Code**	-	-	
128-255	reserve		-	

Appendix: Part Number Table

Product	Advantech PN
SQRAM 8G SO-DDR3L-1600 I-GRD SAM	SQR-SD3I-8G1K6SNLB