SODIMM DDR3L 1600 2GB Datasheet

(SQR-SD3I2G1K6INCCE)

Features:

- **Compliance with**
  - JEDEC Standard 204-pin small-outline dual in-line memory module
  - Intend for PC3-12800 application
  - Backward compatible with PC3-10600 and PC3-8500
  - Bi-Directional Differential Data Strobe
  - 8 Bit pre-fetch, with 8 internal banks for current operation
  - Inputs and Outputs are SSTL-15 compatible
  - DLL aligns DQ and DQS transition with CK transition
  - On-Die Termination (ODT)
  - On-Board EEPROM
  - SDRAM are 96-ball BGA Package
  - RoHS and Halogen free
  - Golden connector

- **SDRAM Configuration:** DDR3L 4Gb 256Mx16 SDRAM

- **Capacities**

  2GB 256Mx64 1 Rank

- **Performance**
  - DDR3L-1600 PC3-12800 CL11
  - DDR3L-1333 PC3-10600 CL9
  - DDR3L-1066 PC3-8500 CL7

- **DRAM Type**
  - DDR3L SODIMM

- **Temperature ranges**

Operating:

  - Industrial: -40°C to 95°C

Storage:

  - -50°C to 100°C

- **Supply voltage**
  - V_{DD}=V_{DDQ}=1.35 Volt
  - V_{DDSPD}=2.25V~2.75V
  -

- **Operation Current**
  - Active mode(max):

    2GB: 1.0 A

    (T_{CASE}: 0°C to 95°C)

- **Form factor**
  - DDR3L 204 Pin SODIMM

- **Certification and Compliance**
  - RoHs
  - REACH
  - CE
  - FCC

Revision History:

Rev.	Description	Date
1.0	Official release	2021/04/21

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1. ADVANTECH Memory Product Description

1.1 Introduction

ADVANTECH Unbuffered Small Outline DDR3L SDRAM DIMMs (Unbuffered Small Outine Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR3L SDRAM devices. These DDR3L SDRAM Unbuffered Small Outline DIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

1.2 Key Parameter

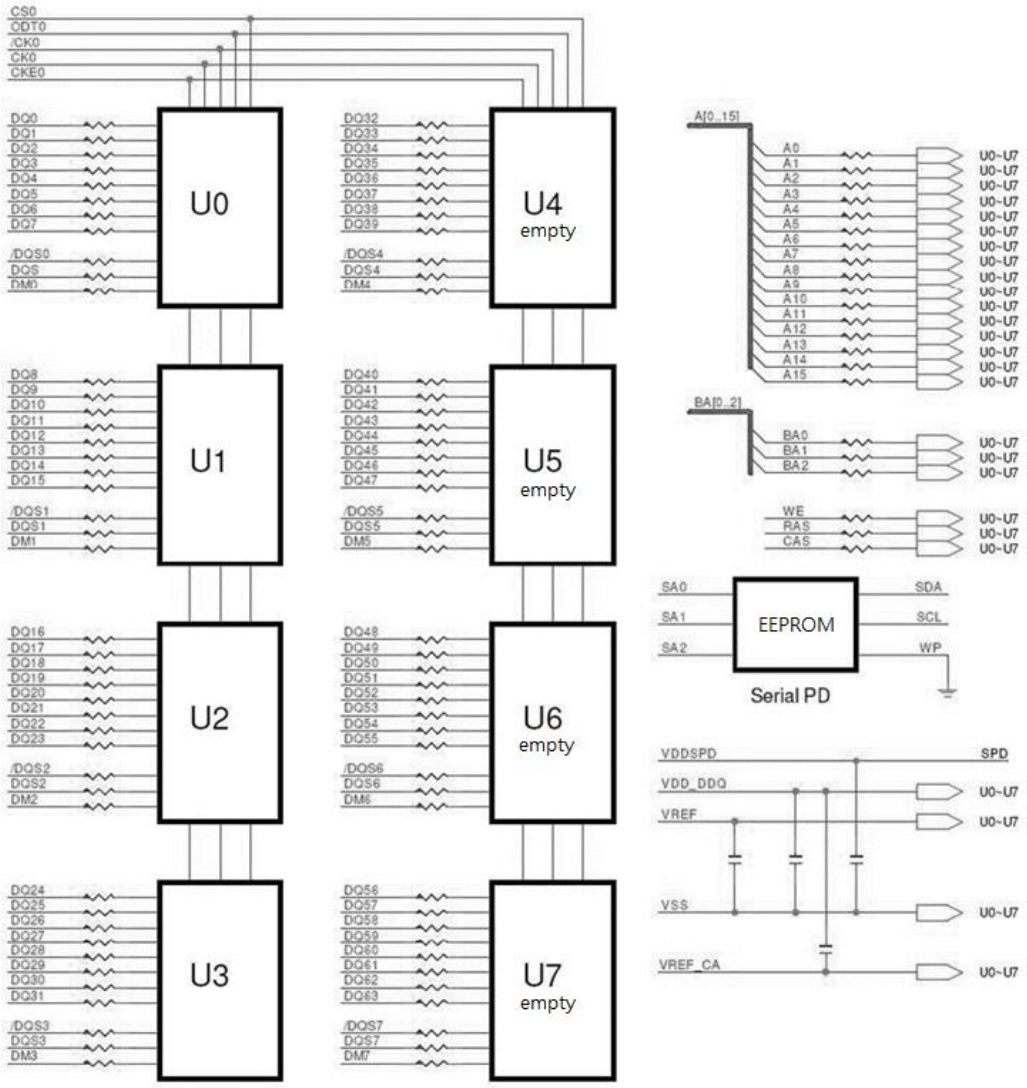
Industry Nomenclature	Data Rate MT/s		tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
	CL=9	CL=11				
PC3-12800	1333	1600	13.75	13.75	35	48.75

1.3 Ordering Information

DDR3L SODIMM					
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank
SQR-SD3I2G1K6INCCE	2GB	PC3-12800	256Mx64	4	1

2. ADVANTECH Memory Module Block Diagram

- DDR3L 2GB, 256Mx16 base, 1Rank



Note:

- The ZQ ball on each DDR3L component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver

3. Environment Requirement

3.1.ADVANTECH DIMM Parameter

ADVANTECH DIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	-40 to +95	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating& storage)	105 to 69	K Pascal	1,2
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR3 DRAM component specification. 2. Up to 9850 ft.				

3.2.SDARM parameter by device density

RTT_Nom Setting	Parameter		4Gb	Units
tREFI	Average periodic refresh interval	0°C≦T_{CASE}≦**85**°C	7.8	μs
		85°C≦T_{CASE}≦**95**°C	3.9	μs

4. Absolute Maximum Rating

4.1.Module Absolut Maximum Rating

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.975	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to +1.975	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to +1.975	V	1
Note: 1. VDDQ tracks with VDD; VDDQ and VDD are tied together.				

4.2.SDRAM Absolut Maximum Rating

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	-40 to 95	℃	1,2
		Extended Temp.(optional)	85 to 95	℃	1,3
T_{STG}	Storage Temperature		-50 to 100	℃	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °Cunder all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all timesand VREF must be not greater than0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

5. Pin Configurations (Front side/Back side)

5.1.Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	2	V_{SS}	69	DQ27	70	DQ31	137	DQS4	138	V_{SS}
3	V_{SS}	4	DQ4	71	V_{SS}	72	V_{SS}	139	V_{SS}	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1	141	DQ34	142	DQ39
7	DQ1	8	V_{SS}	75	V_{DD}	76	V_{DD}	143	DQ35	144	V_{SS}
9	V_{SS}	10	/DQS0	77	NC	78	A15 ***	145	V_{SS}	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14 ***	147	DQ40	148	DQ45
13	V_{SS}	14	V_{SS}	81	V_{DD}	82	V_{DD}	149	DQ41	150	V_{SS}
15	DQ2	16	DQ6	83	A12, /BC	84	A11	151	V_{SS}	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	V_{SS}	20	V_{SS}	87	V_{DD}	88	V_{DD}	155	V_{SS}	156	V_{SS}
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	V_{SS}	26	V_{SS}	93	V_{DD}	94	V_{DD}	161	V_{SS}	162	V_{SS}
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/Reset	97	A1	98	A0	165	DQ49	166	DQ53
31	V_{SS}	32	V_{SS}	99	V_{DD}	100	V_{DD}	167	V_{SS}	168	V_{SS}
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	V_{SS}
37	V_{SS}	38	V_{SS}	105	V_{DD}	106	V_{DD}	173	V_{SS}	174	DQ54
39	DQ16	40	DQ20	107	A10, /AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	V_{SS}
43	V_{SS}	44	V_{SS}	111	V_{DD}	112	V_{DD}	179	V_{SS}	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/S0	181	DQ56	182	DQ61
47	DQS2	48	V_{SS}	115	/CAS	116	ODT0	183	DQ57	184	V_{SS}
49	V_{SS}	50	DQ22	117	V_{DD}	118	V_{DD}	185	V_{SS}	186	/DQS7
51	DQ18	52	DQ23	119	A13 ***	120	ODT1	187	DM7	188	DQS7
53	DQ19	54	V_{SS}	121	/S1	122	NC *	189	V_{SS}	190	V_{SS}
55	V_{SS}	56	DQ28	123	V_{DD}	124	V_{DD}	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST/NC	126	V_{REFCA}	193	DQ59	194	DQ63
59	DQ25	60	V_{SS}	127	V_{SS}	128	V_{SS}	195	V_{SS}	196	V_{SS}
61	V_{SS}	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDD_{SPD}	200	SDA
65	V_{SS}	66	V_{SS}	133	V_{SS}	134	V_{SS}	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	Vtt	204	Vtt

* NC = No Connect
** TEST (PIN# 125) reserve for bus probing, is NC on normal modules.
*** Pin might conneceted to NC ball od DRAMs (depanding on density); alternatively may connect to termination resistor

5.2.Pin Description

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA1	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V_{DD}	Power Supply
/WE	SDRAM write enable	V_{DDID}	V_{DD}Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V_{TT}	SDRAM I/O termination supply.

6. ADVANTECH SDRAM Operation Condition

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.283	1.35	1.45	V	1,2
V_{DDQ}	Supply Voltage	1.283	1.35	1.45	V	1,2
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$	DC Input High (Logic1) Voltage	V_{REF} + 0.1	-	V_{DD}	V	3
$V_{IL\ (DC)}$	DC Input Low (Logic0) Voltage	V_{SS}	-	V_{REF} - 0.1	V	3
$V_{IH\ (AC)}$	AC Input High (Logic1) Voltage	V_{REF}+ 0.175	-	-	V	3
$V_{IL\ (AC)}$	AC Input Low (Logic0) Voltage	-	-	V_{REF} - 0.175	V	3
$V_{REFDQ\ (DC)}$	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
$V_{REFCA\ (DC)}$	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC output Levels						
$V_{OH\ (DC)}$	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
$V_{OH\ (AC)}$	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)}$	Differential Input high ac	$2*(V_{IH\ (AC)}-V_{REF})$	-	Note 9	V	8
$V_{ILdiff(ac)}$	Differential Input logic Low ac	Note 9	-	$2*(V_{REF}- V_{IL\ (AC)})$	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
5. For reference: approx. VDD/2 +/- 15 mV.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high orlow swing with a driver impedance of 40 Ωand an effective test load of 25 Ωto V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high orlow swing with a driver impedance of 40 Ωand an effective test load of 25 Ωto V_{TT} = V_{DDQ}/2 ateach of the differential outputs.

7. Operating, Standby and Refresh Currents

- **2GB SODIMM** (1Rank 256Mx16 DDR3L SDRAMs)

Symbol	Parameter/Condition	PC3-12800	Unit
I DD0	One bank; Active - Precharge	160	mA
I DD1	One bank; Active - Read - Precharge	200	mA
I DD2N	Precharge Standby Current	72	mA
I DD2P	Precharge Power Down Current	48	mA
I DD2Q	Pecharge Quiet Standby Current	72	mA
I DD3N	Active Standby Current	132	mA
I DD3P	Active Power-Down Current	96	mA
I DD4R	Operating Current Burst Read	520	mA
I DD4W	Operating Current Burst Write	520	mA
I DD5B	Burst Refresh Current	520	mA
I DD6	Self-Refresh Current: Normal Temperature Range	52	mA
I DD7	Operating Bank Interleave Read Current	740	mA

8. Serial Presence Detect

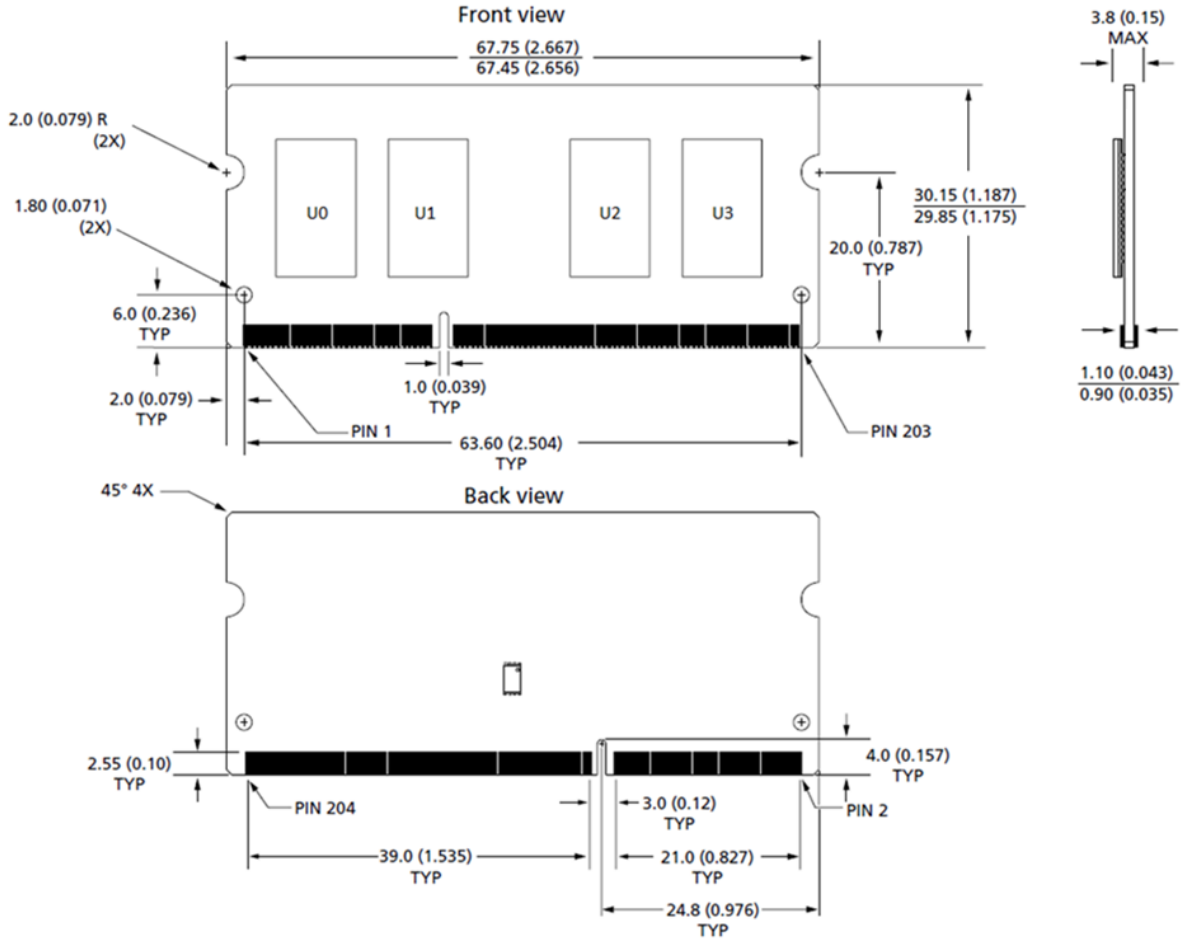
- SQR-SD3I2G1K6INCCE

Byte	Description	Function support	Byte Value
0	Number of Serial PD Bytes Written during Production	116/256/176 Bytes	92
1	SPD Revision	1.3	13
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte/Module type	SO DIMM	03
4	SDRAM Density and Banks	8 banks, 4Gb	04
5	SDRAM Address	15/10	19
6	Reserve	1.35V/1.5V Operable	02
7	Module Organization	1rank/x16	02
8	Module Memory Bus Width	64bit bus	03
9	Fine Timebase (FTB) Dividend/Divisor	-	11
10	Medium Timebase (MTB) Dividend	1ns	01
11	Medium Timebase (MTB) Divisor	8	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserve	Blank	00
14	CAS latency, least Significant Byte	5, 6,7,8,9,10,11	FE
15	CAS latency, most Significant Byte	Not support over CL12	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns	3C
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	Refer to Byte22,23	11
22	Minimum Active to Precharge Delay Time (tRASmin), Least SignificantByte	35ns	18
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least SignificantByte	48.125ns	81

24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260 ns	20
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260 ns	08
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	Refer to Byte29	01
29	Minimum Four Activate Window Delay Time (tFAWmin)	40 ns	40
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ASR, Normal Temp	01
32	Module Thermal Sensor	Thermal Sensor supported	80
33-40	Reserve	Blank	00
41	tMAW, MAC	8K*tREFI / Unlimited	88
34-59	Reserve	Blank	00
60	Module Nominal Height of Unbuffered DIMM	30.00	0F
61	Module Maximum Thickness of Unbuffered DIMM	1.2/1.2	11
62	Reference Raw Card Revision	A1	20
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-117	Reserve	Blank	00
117-118	Module Manufacturer's JEDEC ID Code	Advantech	8A C8
119	Module Manufacturing Location	Taiwan	02
120-121	Module Manufacturing Date	Variable	-
126-127	Cyclical Redundancy Code	CRC cover 0~116 byte	7B 22
128-145	Module Part Number	SQR-SD3I2G1K6INCCE	53 51 52 2D 53 44 33 49 32 47 31 4B 36 49 4E 43 43 45
146-147	Module Revision Code	-	00 10
148-149	DRAM Manufacturer JEDEC ID Code	ISSI	01 9D
150-255	Reserve	Blank	-

9. Package Dimension

-2GB DDR3L SODIMM, 256Mx64, 1 Rank



Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

2. The dimensional diagram is for reference only.

10. Reliability Specifications

10.1. Environmental Conditions

Environment	Specification
Storage Temperature	-50°C ~ +100°C
Operating Temperature	-40℃ to 95℃ (Industrial)