

SODIMM DDR3L 1866 8GB

Datasheet

(SQR-SD3M-8G1K8SNLB)

CONTENTS

1. Description.....	4
2. Features	4
3. Dimension	5
4. Pin Identification	6
5. Pin Configurations	7
6. Block Diagram	8
7. Parameter & Operating Conditions	9
Appendix: Part Number Table	19

Revision History

Rev	Date	Modification
1.0	16 th Jan., 2017	Official released.

Advantech reserves the right to make changes without further notice to any products or data herein to improve reliability, function, or design. Information furnished by Advantech is believed to be accurate and reliable. However, Advantech does not assure any liability arising out of the application or use of this information, nor the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.

Copyright © 1983-2011 Advantech Co., Ltd. All rights reserved.

1. Description

The SQR-SD3M-8G1K8SNLB is a 1G x 64bits DDR3L-1866 2Rank SO-DIMM. It consists of 16pcs 512Mx8bits DDR3L SDRAMs FBGA packages and a 2048 bits serial EEPROM on a 204-pin printed circuit board. The SQR-SD3M-8G1K8SNLB is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. Features

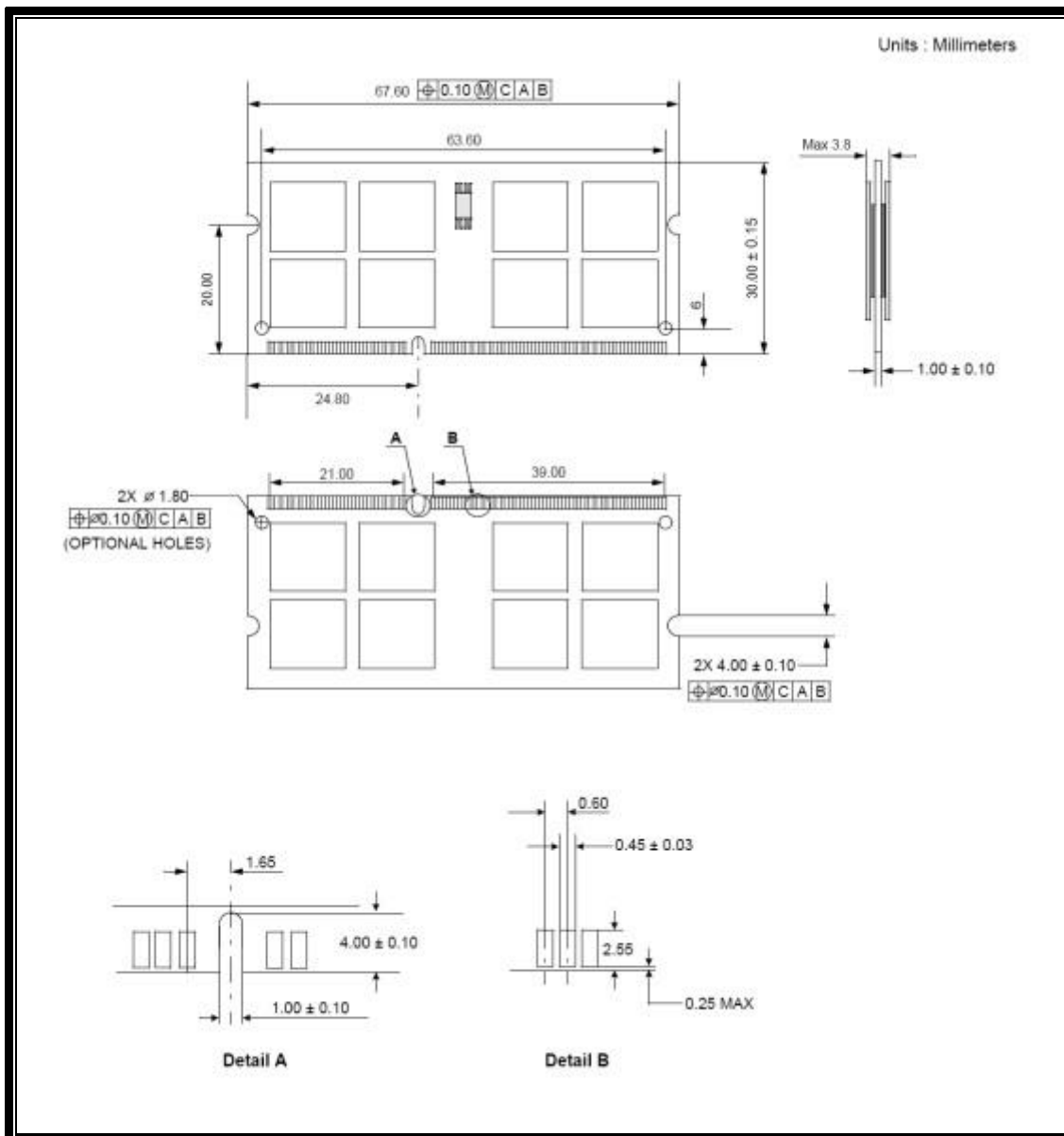
- Key Parameter

Industry Nomenclature	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
	CL=9	CL=11	CL=13			
PC3-14900	1333	1600	1866	13.125	13.125	13.125

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-14900 applications
- **CL-tRCD-tRP: 13-13-13**
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (-0.067V/+0.1V) or 1.5Volt (-0.1V/+0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- On-Board thermal sensor (Class B)
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (TA ≤ +85°C)
- 16/10/1 Addressing (row/column/rank)-8GB
- Golden Connector (Au: 30μ")
- SDRAM operating temperature range -20°C ≤ TCASE ≤ +85°C
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 7, 9, 11, 13
 - Burst Length: switch on-the-fly: BL=8 or BC 4

3. Dimension

(8GB, 2 Rank 512Mx8 DDR3L base SODIMM)



Note: Device position is only for reference.

4. Pin Identification

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	VDD	Power Supply
/WE	SDRAM write enable	VDDID	VDD Identification Flag
/S0 - /S1	DIMM Rank Select Lines	VDDQ	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	VREFDQ	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	VREFCA	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	VSS	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	VDDSPD	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	VTT	SDRAM I/O termination supply.

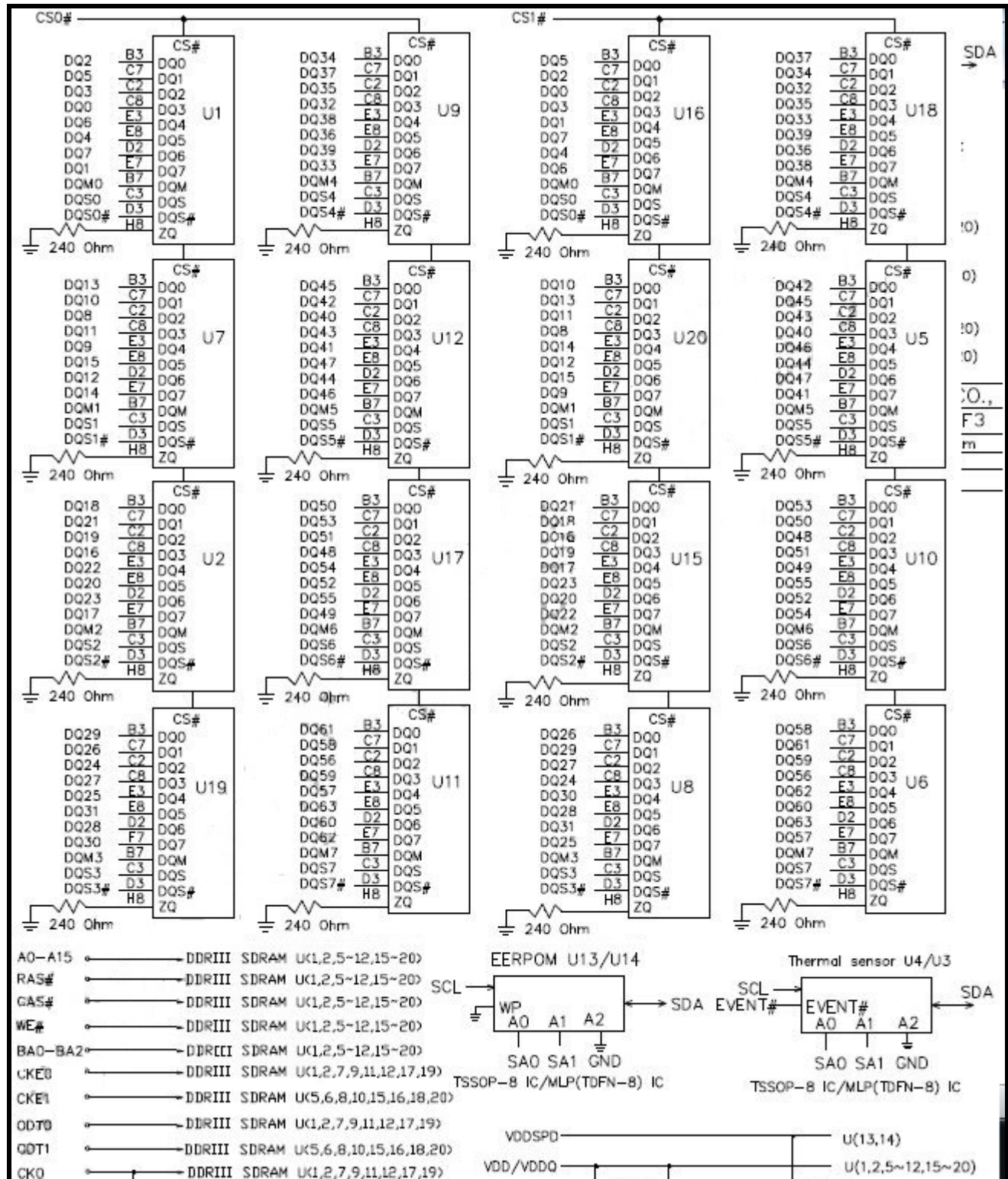
5. Pin Configurations

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	2	VSS	69	DQ27	70	DQ31	137	DQS4	138	VSS
3	VSS	4	DQ4	71	VSS	72	VSS	139	VSS	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1	141	DQ34	142	DQ39
7	DQ1	8	VSS	75	VDD	76	VDD	143	DQ35	144	VSS
9	VSS	10	/DQS0	77	NC	78	A15 ***	145	VSS	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14 ***	147	DQ40	148	DQ45
13	VSS	14	VSS	81	VDD	82	VDD	149	DQ41	150	VSS
15	DQ2	16	DQ6	83	A12, /BC	84	A11	151	VSS	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	VSS	20	VSS	87	VDD	88	VDD	155	VSS	156	VSS
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	VSS	26	VSS	93	VDD	94	VDD	161	VSS	162	VSS
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/Reset	97	A1	98	A0	165	DQ49	166	DQ53
31	VSS	32	VSS	99	VDD	100	VDD	167	VSS	168	VSS
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	VSS
37	VSS	38	VSS	105	VDD	106	VDD	173	VSS	174	DQ54
39	DQ16	40	DQ20	107	A10, /AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	VSS
43	VSS	44	VSS	111	VDD	112	VDD	179	VSS	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/S0	181	DQ56	182	DQ61
47	DQS2	48	VSS	115	/CAS	116	ODT0	183	DQ57	184	VSS
49	VSS	50	DQ22	117	VDD	118	VDD	185	VSS	186	/DQS7
51	DQ18	52	DQ23	119	A13 ***	120	ODT1	187	DM7	188	DQS7
53	DQ19	54	VSS	121	/S1	122	NC *	189	VSS	190	VSS
55	VSS	56	DQ28	123	VDD	124	VDD	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST/NC	126	VREFCA	193	DQ59	194	DQ63
59	DQ25	60	VSS	127	VSS	128	VSS	195	VSS	196	VSS
61	VSS	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDDSPD	200	SDA
65	VSS	66	VSS	133	VSS	134	VSS	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	Vtt	204	Vtt

* NC = No Connect
 ** TEST (PIN# 125) reserve for bus probing, is NC on normal modules.
 *** Pin might conneced to NC ball od DRAMs (depanding on density); alternatively may connect to termination resistor

6. Block Diagram

(8GB, 2Rank, 512Mx8 DDR3L SDRAMs)



7. Parameter & Operating Conditions

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating Temperature	TCASE	-20 to +85	°C	1,2
Note: 1. Operating Temperature Tcase is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2. 2. At -20 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.				

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on VDD relative to Vss	VDD	-0.4 to +1.975	V	1,3
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4 to +1.975	V	1,3
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 to +1.975	V	1
Storage temperature	TSTG	-55 to 150	°C	1,2
Note: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard. 3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV				

AC & DC Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDQ	Supply Voltage	1.283	1.35	1.45	V	1,2
Single Ended AC/DC Input Levels						
VIH (DC)	DC Input High (Logic1) Voltage	VREF + 0.1	-	VDD	V	3
VIL (DC)	DC Input Low (Logic 0) Voltage	VSS	-	VREF - 0.1	V	3
VIH (AC)	AC Input High (Logic1) Voltage	VREF+ 0.175	-	-	V	3
VIL (AC)	AC Input Low (Logic 0) Voltage	-	-	VREF - 0.175	V	3
VREFDQ (DC)	Reference Voltage for DQ, DM inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
VREFCA (DC)	Reference Voltage for ADD,CMD inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
Single Ended AC/DC output Levels						
VOH (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
VOM (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
VOL (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	

VOH (AC)	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times V_{DDQ}$	-	V	6
VOL (AC)	AC output low measurement level (for output SR)		$V_{TT} - 0.1 \times V_{DDQ}$	-	V	6
Differential AC/DC Input Levels						
VIHdiff	Differential Input high	+0.2	-	Note 9	V	7
VILdiff	Differential Input logic Low	Note 9	-	-0.2	V	7
VIHdiff(ac)	Differential Input high ac	$2 \times (V_{IH} (AC) - V_{REF})$	-	Note 9	V	8
VILdiff(ac)	Differential Input logic Low ac	Note 9	-	$2 \times (V_{REF} - V_{IL} (AC))$	V	8
Differential AC and DC Output Levels						
VOHdiff(AC)	AC differential output high measurement level (for output SR)	-	$+ 0.2 \times V_{DDQ}$	-	V	10
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-	$- 0.2 \times V_{DDQ}$	-	V	10

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA.
- The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
- For reference: approx. VDD/2 +/- 15 mV.
- The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$
- Used to define a differential signal slew-rate.
- For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.
- The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

Operating, Standby, and Refresh Currents

- 8GB SODIMM (2 Rank, 512Mx8 DDR3L SDRAMs TCASE = -20 °C ~ 85 °C)

Symbol	Parameter/Condition		PC3-14900	Unit
I DD0	One bank; Active - Precharge		480	mA
I DD1	One bank; Active - Read - Precharge		720	mA
I DD2N	Precharge Standby Current		224	mA
IDD2NT	Precharge Standby ODT Current		256	mA
I DD2P	Precharge Power Down Current	Fast Mode	176	mA
	Precharge Power Down Current	Slow Mode	176	mA
I DD2Q	Precharge Quiet Standby Current		208	mA
I DD3N	Active Standby Current		368	mA
I DD3P	Active Power-Down Current		176	mA
I DD4R	Operating Current Burst Read		1232	mA
I DD4W	Operating Current Burst Write		1216	mA
I DD5B	Burst Refresh Current		3120	mA
I DD6	Self-Refresh Current: Normal Temperature Range		240	mA
I DD7	Operating Bank Interleave Read Current		2160	mA
I DD8	RESET Low Current		240	mA

Timing Parameters & Specifications

(TCASE = -20 °C ~ 85 °C; VDDQ = VDD , See AC Characteristics)

Parameter	Symbol	PC3-14900		Unit
		Min.	Max.	
Clock Timing				
Minimum Clock Cycle Time	tCK (DLL-Off)	8	-	ns
Average Clock Period	tCK (avg)	1.071	<1.25	ns
Average high pulse width	tCH (avg)	0.47	0.53	tCK (avg)
Average low pulse width	tCL (avg)	0.47	0.53	tCK (avg)
Absolute Clock Period	tCK (abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max -	Ps
Absolute high pulse width	tCH (abs)	0.43	-	tCK (avg)
Absolute low pulse width	tCL (abs)	0.43	-	tCK (avg)
Clock Period Jitter	JIT (per)	-60	60	Ps
Clock Period Jitter during DLL locking period.	TJIT (per, lck)	-50	50	Ps
Cycle to Cycle Period Jitter	JIT (CC)	120		
Cycle to Cycle Period Jitter during DLL locking period.	TJIT (CC, lck)	100		
	TJIT (duty)	-	-	Ps
Cumulative error across 2 cycle	TERR (2per)	-88	88	Ps
Cumulative error across 3 cycle	TERR (3per)	-105	105	Ps
Cumulative error across 4 cycle	TERR (4per)	-117	117	Ps
Cumulative error across 5 cycle	TERR (5per)	-126	126	Ps
Cumulative error across 6 cycle	TERR (6per)	-133	133	Ps
Cumulative error across 7 cycle	TERR (7per)	-139	139	Ps
Cumulative error across 8 cycle	TERR (8per)	-145	145	Ps
Cumulative error across 9 cycle	TERR (9per)	-150	150	Ps
Cumulative error across 10 cycle	TERR (10per)	-154	154	Ps
Cumulative error across 11 cycle	TERR (11per)	-158	158	Ps
Cumulative error across 12 cycle	TERR (12per)	-161	161	Ps
Cumulative error across 13~50 cycle	TERR (nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max =		

		(1 + 0.68ln(n)) * tJIT(per)max		
Data Timing				
Parameter	Symbol	Min.	Max.	Unit
DQS, DQS# to DQ skew, per group, per access	tDSQ	-	85	Ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ (DQ)	-390	195	Ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	195	Ps
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	68	-	Ps
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	-	-	Ps
Data Strobe Timing				
Parameter	Symbol	Min.	Max.	Unit
DQS,DQS# differential READ Preamble	tRPRE	0.9		tCK(avg)
DQS, DQS# differential READ Postamble	tRPST	0.3		tCK(avg)
DQS, DQS# differential output high time	tQSH	0.4		tCK(avg)
DQS, DQS# differential output low time	tQSL	0.4		tCK(avg)
DQS, DQS# differential WRITE Preamble	tWPRE	0.9		tCK(avg)
DQS, DQS# differential WRITE Postamble	tWPST	0.3		tCK(avg)
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-195	195	Ps
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-390	195	Ps
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	195	Ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	tCK(avg)

DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	tCK(avg)
Command and Address Timing				
Parameter	Symbol	Min.	Max.	Unit
DLL locking time	tDLLK	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to Internal read command	tWTR	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	
Refer to Section 1 Feature	tRCD	Refer to Section 1 Feature		
Refer to Section 1 Feature	tRP	Refer to Section 1 Feature		
Refer to Section 1 Feature	tRC	Refer to Section 1 Feature		
	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL (min)	WR + roundup(tRP / tCK(avg))		nCK
Multi-Purpose Register Recovery Time	tMPRR	1		nCK
ACTIVE to PRECHARGE command period	tRAS	34	9 tREFI	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 5ns)		
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 6ns)		
Four activate window for 1KB page size	tFAW	27		ns
Four activate window for 2KB page size	tFAW	35	-	ns
Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	tIS (base)	65		ns
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	100		ps
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	150		ps
Calibration Timing				

Parameter	Symbol	Min.	Max.	Unit
Power-up and RESET calibration time	tZQinit	Max. (512nCK, 640ns)	-	nCK
Normal operation Full calibration time	tZQoper	Max. (256nCK, 320ns)	-	nCK
Normal operation Short calibration time	tZQCS	Max. (64nCK, 80ns)	-	nCK
Reset Timing				
Parameter	Symbol	Min.	Max.	Unit
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				
Parameter	Symbol	Min.	Max.	Unit
Exit Self Refresh to commands not requiring a locked DLL	tXS	Max(5nCK, tRFC(min)+10ns)		
Exit Self Refresh to commands requiring a locked DLL.	tXSDLL	tDLL(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing.	tCKESR	tCKE9min)+1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max(5nCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	Max(5nCK, 10ns)	-	
Power Down Timings				
Parameter	Symbol	Min.	Max.	Unit
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	
Command pass disable delay	tCPDED	2	-	nCK
Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK

Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 +(tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 +WR + 1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 +(tWR /tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 +WR + 1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	nCK
ODT Timings				
Parameter	Symbol	Min.	Max.	Unit
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
RTT-turn-on	tAON	-195	195	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
Parameter	Symbol	Min	Max	Unit
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	140	-	ps
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	140	-	ps
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

SERIAL PRESENCE DETECT SPECIFICATION

2 RANK SODIMM DIMM based on 512Mx8, 8Banks, 8K Refresh, DDR3L SDRAMs with SPD

Byte	Description	Function Supported	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	112/256/176 Bytes	92	
1	SPD Revision	SPD Revision 1.2	13	
2	Key Byte/DRAM Device Type	DDR3-DRAM	0B	
3	Key Byte/Module type	SODIMM	03	
4	SDRAM Density and Banks	8 Banks, 8GB	04	
5	SDRAM Address	16/11	21	
6	Reserve	1.35V Operable	02	
7	Module Organization	1 Rank x8	09	
8	Module Memory Bus Width	64bit Bus	03	
9	Fine Timebase (FTB) Dividend/Divisor	DDR3-Fine Timebase Dividend/Divisor	11	
10	Medium Timebase (MTB) Dividend	1ns	01	
11	Medium Timebase (MTB) Divisor	8	08	
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3-Min SDRAM Cycle Time	09	
13	Reserve	Reserved	00	
14	CAS latency, least Significant Byte	DDR3-CAS LATENCIES SUPPORTED	FE	
15	CAS latency, most Significant Byte	DDR3-CAS LATENCIES SUPPORTED	02	
16	Minimum CAS Latency Time (tAmin)	13.125ns	69	
17	Minimum Write Recovery Time (tWRmin)	15ns	78	
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	DDR3-MIN ROW ACTIVE TO ROW ACTIVE DELAY	28	
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69	
21	Upper Nibbles for tRAS and tRC	Refer to Byte 22,23	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	34ns	10	

23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	47.5ns	79	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260ns	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260ns	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C	
28	Upper Nibble for tFAW	Refer Byte 29	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	DDR3-MIN FOUR ACTIVE WINDOW DELAY	D8	
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83	
31	SDRAM Thermal and Refresh Options	DDR3-SDRAM DEVICE THERMAL REFRESH OPTIONS	01	
32	Module Thermal Sensor	Thermal Sensor	80	
33	SDRAM Device Type	Mono-Die	00	
34-59	Reserve	Reserve	00	
60-63	Module Type Specific Section,	-	0F 11 25 00	
64-117	Reserve	-	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Innodisk	86 F1	
119	Module ID: Module Manufacturing Location	-	02	
120-121	Module ID: Module Manufacturing Date	-	00 00	
122-125	Module Serial Number	-	00	
126-127	SPD Cyclical Redundancy Code	-	-	
128-255	reserve		-	

Appendix: Part Number Table

Product	Advantech PN
SGRAM 8G SO-DDR3L-1866 M-GRD	SQR-SD3M-8G1K8SNLB