

SODIMM DDR3L 1600 8GB

Datasheet

(SQR-SD3N8G1K6MNEPB)

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Revision History

Rev	Date	Modification
1.0	30 TH Apr., 2020	Official released.

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1. Features

● Key Parameter

Industry Nomenclature	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
	CL=7	CL=9	CL=11			
PC3-12800	1066	1333	1600	13.125	13.125	13.125

Micron 512x8 P-die

- JEDEC Standard 204-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- CL-tRCD-tRP: 11-11-11
- VDD=VDDQ= 1.35 Volt (-0.067V/+0.1V) or 1.5Volt (-0.1V/+0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- On-Board thermal sensor
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (Tc ≤ +85°C)
- 16/10/1 Addressing (row/column/rank)-8GB
- Golden Connector (Au: 30μ")
- SDRAM operating temperature range 0°C ≤ TCASE ≤ +85°C
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 6,7,8,9,10,11
 - Burst Length: switch on-the-fly: BL=8 or BC 4

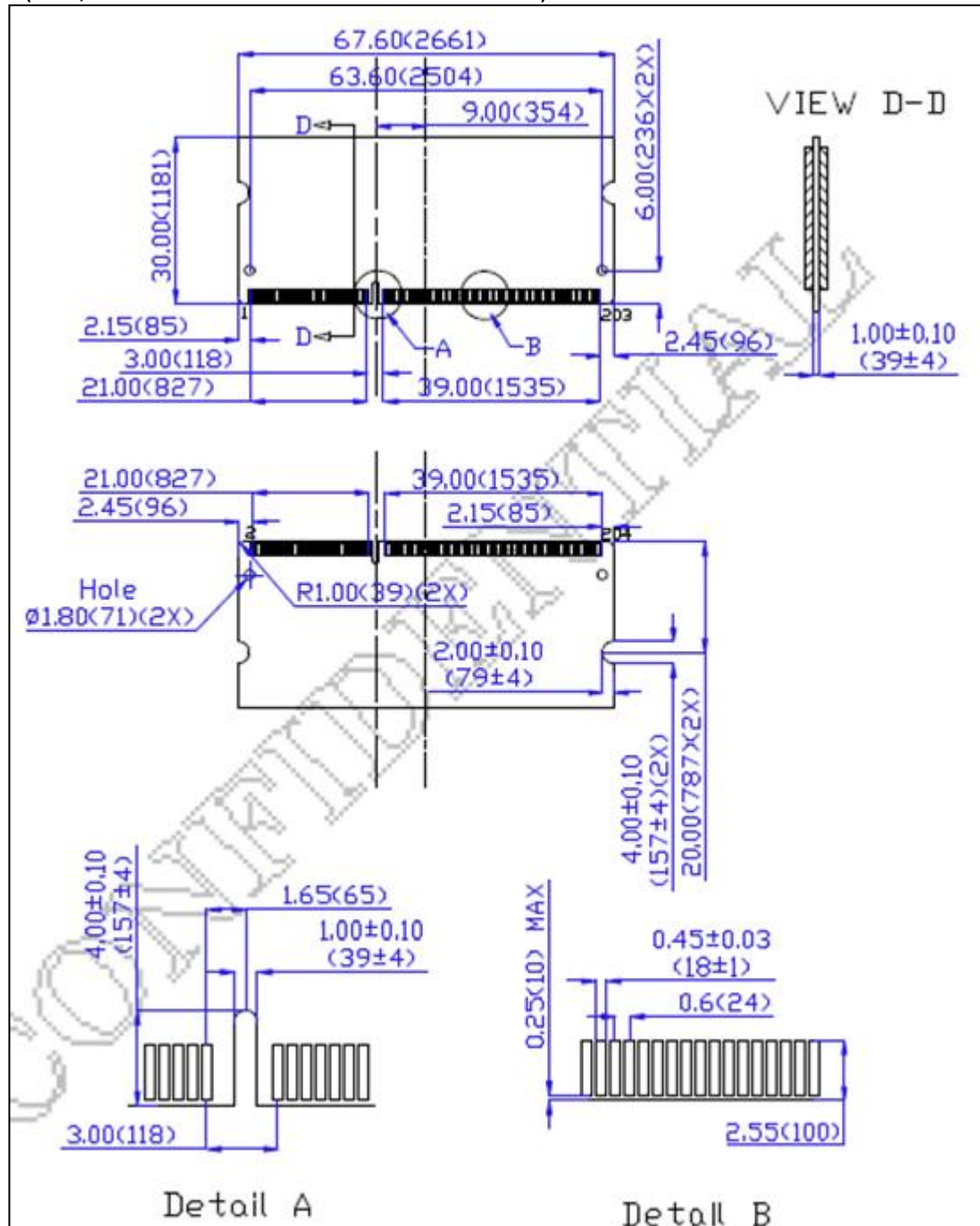
2. Order Information

Extend Temperature DDR3L SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	Thermal Sensor
SQR-SD3N8G1K6MNEPB	8GB	PC3-12800	1Gx64	16	2	Y

IC: Micron: 512Mx8 P-die

3. Dimension

(8GB, 2 Ranks 512Mx8 DDR3L base SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

4. Pin Identification

Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
/CK[1:0]	Clock inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
/RAS	Row Address Strobe	1	/DQS[7:0]	Data strobes complement	8
/CAS	Column Address Strobe	1	/RESET	Reset Pin	1
/WE	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SO-DIMM)	1
/S[1:0]	Chip Selects	2	/EVENT	Temperature event pin	1
A[9:0],A11,A[15:13]	Address Inputs	14	VDD	Core and I/O Power	18
A10,AP	Address Input/Autoprecharge	1	VSS	Ground	52
A12,/BC	Address Input/Burst chop	1			
BA[2:0]	SDRAM Bank Address	3	VREFDQ, VREFCA	Input/Output Reference	2
ODT[1:0]	On-die termination control	2	VDDSPD	SPD and Temp sensor Power	1
SCL	Serial Presence Detect (SPD) and Thermal sensor(TS) Clock Input	1	Vtt	Termination voltage	2
SDA	SPD and TS Data Input/Output	1	NC	Reserved for future use	2
SA[1:0]	SPD and TS address	2		Total:	204

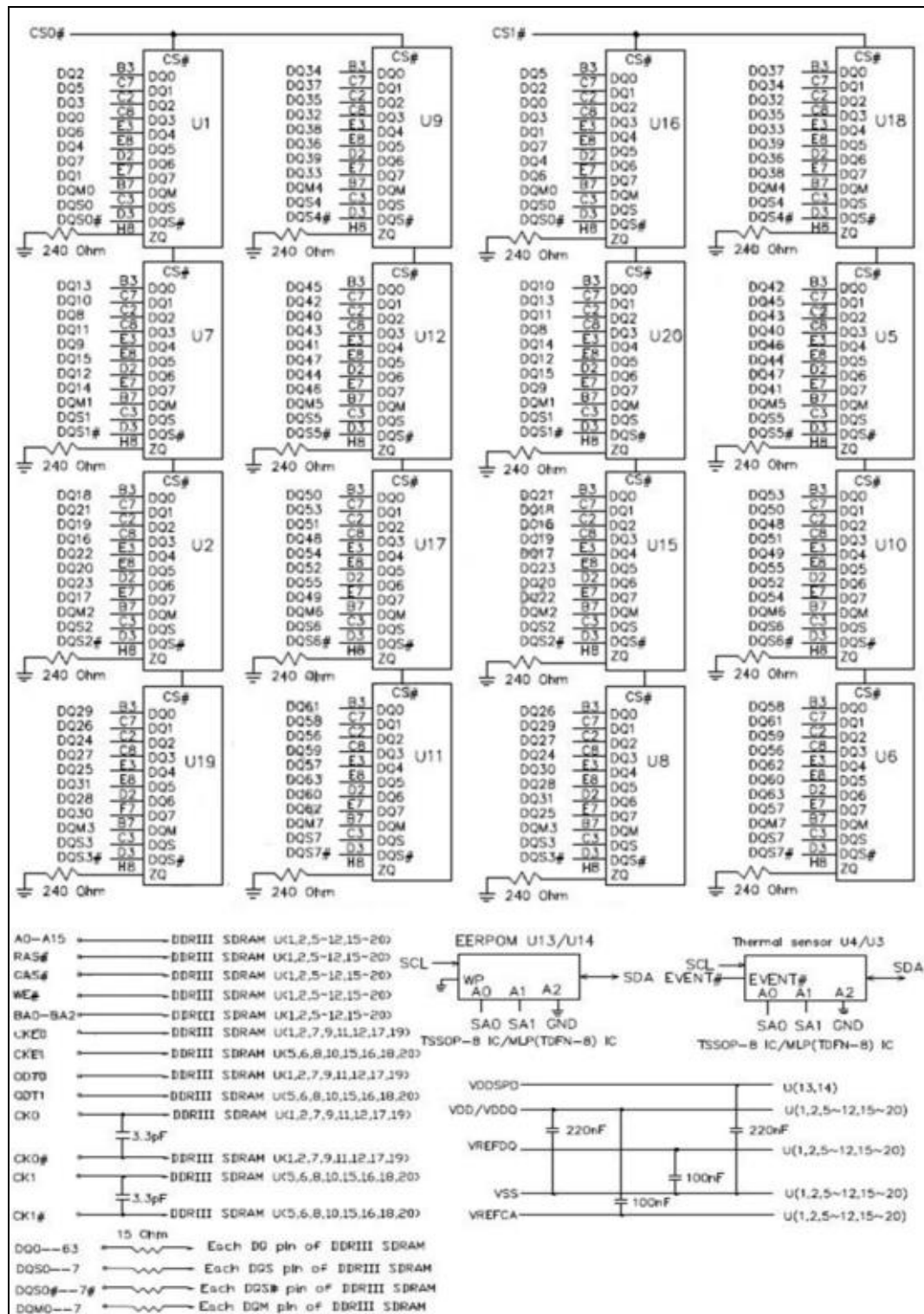
5. Pin Configurations

Front						Back					
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	69	DQ27	137	DQ34	2	VSS	70	DQ31	138	VSS
3	VSS	71	VSS	139	VSS	4	DQ4	72	VSS	140	DQ38
5	DQ0	73	CKE0	141	DQ34	6	DQ5	74	CKE1	142	DQ39
7	DQ1	75	VDD	143	DQ35	8	VSS	76	VDD	144	VSS
9	VSS	77	NC	145	VSS	10	/DQ30	78	A13*	146	DQ44
11	DM0	79	BA2	147	DQ40	12	DQ30	80	A14*	148	DQ45
13	VSS	81	VDD	149	DQ41	14	VSS	82	VDD	150	VSS
15	DQ2	83	A12, /B/C	151	VSS	16	DQ6	84	A11	152	/DQ35
17	DQ3	85	A8	153	DM3	18	DQ7	86	A7	154	DQ55
19	VSS	87	VDD	155	VSS	20	VSS	88	VDD	156	VSS
21	DQ8	89	A8	157	DQ42	22	DQ12	90	A6	158	DQ46
23	DQ9	91	A5	159	DQ43	24	DQ13	92	A4	160	DQ47
25	VSS	93	VDD	161	VSS	26	VSS	94	VDD	162	VSS
27	/DQ51	95	A3	163	DQ48	28	DM1	96	A2	164	DQ52
29	DQ51	97	A1	165	DQ49	30	/RESET	98	A0	166	DQ53
31	VSS	99	VDD	167	VSS	32	VSS	100	VDD	168	VSS
33	DQ10	101	CK0	169	/DQ56	34	DQ14	102	CK1	170	DM6
35	DQ11	103	/CK0	171	DQ56	36	DQ15	104	/CK1	172	VSS
37	VSS	105	VDD	173	VSS	38	VSS	106	VDD	174	DQ54
39	DQ16	107	A10, /AF	175	DQ50	40	DQ20	108	BA1	176	DQ55
41	DQ17	109	BA0	177	DQ51	42	DQ21	110	/RAS	178	VSS
43	VSS	111	VDD	179	VSS	44	VSS	112	VDD	180	DQ60
45	/DQ52	113	/WE	181	DQ56	46	DM2	114	/SD	182	DQ61
47	DQ52	115	/CAS	183	DQ57	48	VSS	116	ODT0	184	VSS
49	VSS	117	VDD	185	VSS	50	DQ22	118	VDD	186	/DQ57
51	DQ18	119	A13*	187	DM7	52	DQ23	120	ODT1	188	DQ57
53	DQ19	121	/S1	189	VSS	54	VSS	122	NC	190	VSS
55	VSS	123	VDD	191	DQ58	56	DQ28	124	VDD	192	DQ62
57	DQ24	125	NC	193	DQ59	58	DQ29	126	VREFCA	194	DQ63
59	DQ25	127	VSS	195	VSS	60	VSS	128	VSS	196	VSS
61	VSS	129	DQ32	197	SA0	62	/DQ53	130	DQ36	198	/EVENT, N F
63	DM3	131	DQ33	199	VDDSPD	64	DQ53	132	DQ37	200	SDA
65	VSS	133	VSS	201	SA1	66	VSS	134	VSS	202	SCL
67	DQ26	135	/DQ54	203	VTT	68	DQ30	136	DM4	204	VTT

* This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

6. Block Diagram

(8GB, 2 Ranks 512Mx8 DDR3L SDRAMs)



Specifications subject to change without notice, contact your sales representatives for the most update information.

7. Parameter & Operating Conditions

Environmental Requirements

DDR3L W/T SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

.Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +85	°C	3
HOPR	Operating Humidity (relative)	10 to 90	%	
TSTG	Storage Temperature	-50 to +100	°C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Note 2 Up to 9850 ft. Note 3 The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR3L DRAM component specification. Following JEDEC specifications.				

DRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tRFC	REF command ACT or REF command time		260	ns
tREFI	Average periodic refresh interval	$0^{\circ}\text{C} \leq \text{TCASE} \leq 85^{\circ}\text{C}$	7.8	μs
		$85^{\circ}\text{C} \leq \text{TCASE} \leq 95^{\circ}\text{C}$	3.9	μs

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{CASE}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-50 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Industrial Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 to 85 °C under all operating conditions.
- Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
Recommended DC Operating Conditions - DDR3L (1.35V) operation						
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
VDDQ	Supply Voltage	1.283	1.35	1.45	V	1,2
Recommended DC Operating Conditions - DDR3 (1.5V) operation						
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
VDDQ	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
VIH (DC) DDR3L	DC Input High (Logic1) Voltage	+ 90	-	VDD	mV	3
VIH (DC) DDR3	DC Input High (Logic1) Voltage	+ 90		VDD	mV	3
VIL (DC) DDR3L	DC Input Low (Logic 0) Voltage	VSS	-	- 90	mV	3
VIL (DC) DDR3	DC Input Low (Logic 0) Voltage	VSS		- 90	mV	3
VIH (AC) DDR3L	AC Input High (Logic1) Voltage	+ 135	-	-	mV	3
VIH (AC) DDR3	AC Input High (Logic1) Voltage	+ 135			mV	3
VIL (AC) DDR3L	AC Input Low (Logic 0) Voltage	-	-	- 135	mV	3
VIL (AC) DDR3	AC Input Low (Logic 0) Voltage			- 135	mV	3
VREFDQ (DC)	Reference Voltage for DQ, DM inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
VREFCA (DC)	Reference Voltage for ADD,CMD inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
Single Ended AC/DC Output Levels						
VOH (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
VOM (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
VOL (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
VOH (AC)	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
VOL (AC)	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6
Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
VIHdiff DDR3L	Differential Input high	+0.18	-	Note 9	V	7
VIHdiff DDR3	Differential Input high	+0.2		Note 9	V	7

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VILdiff DDR3L	Differential Input logic Low	Note 9	-	-0.18	V	7
VILdiff DDR3	Differential Input logic Low	Note 9	-	-0.2	V	7
VIHdiff(ac) DDR3L	Differential Input high ac	2* (VIH (AC)-VREF)	-	Note 9	V	8
VIHdiff(ac) DDR3	Differential Input high ac	2* (VIH (AC)-VREF)	-	Note 9	V	8
VILdiff(ac) DDR3L	Differential Input logic Low ac	Note 9	-	2* (VREF- VIL (AC))	V	8
VILdiff(ac) DDR3	Differential Input logic Low ac	Note 9	-	2* (VREF- VIL (AC))	V	8
Differential AC and DC Output Levels						
VOHdiff(AC)	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
VOLDiff(AC)	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10
Note: - Under all conditions VDDQ must be less than or equal to VDD. - VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together. - For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA. - Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV) - For reference: approx. VDD/2. - The swing of $\pm 0.1 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2 - Used to define a differential signal slew-rate. - For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here. - These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot. - The swing of $\pm 0.2 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to VTT = VDDQ/2 at each of the differential outputs.						

Operating, Standby, and Refresh Currents

- 8GB SODIMM (2 Ranks, 512Mx8 DDR3L SDRAMs)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active - Precharge		448	mA
I DD1	One bank; Active - Read - Precharge		688	mA
I DD2N	Precharge Standby Current		256	mA
I DD2P	Precharge Power Down Current	Fast Mode	176	mA
	Precharge Power Down Current	Slow Mode	160	mA
I DD2Q	Precharge Quiet Standby Current		240	mA
I DD3N	Active Standby Current		320	mA
I DD3P	Active Power-Down Current		240	mA
I DD4R	Operating Current Burst Read		1440	mA
I DD4W	Operating Current Burst Write		1440	mA
I DD5B	Burst Refresh Current		2432	mA
I DD6	Self-Refresh Current: Normal Temperature Range		240	mA
I DD7	Operating Bank Interleave Read Current		2080	mA
I DD8	RESET Low Current		IDD2P + 2mA	mA

Timing Parameters & Specifications

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.25	<1.5	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps
TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	Parameter	Min.	Max.	Unit
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
1.35V				

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tDS(base) AC160	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC135		25	-	Ps
tDS(base) AC125		-	-	Ps
tDH(base) DC90	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	55	-	Ps
1.5V				
tDS(base) AC175	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC150		10	-	Ps
tDS(base) AC135		-	-	Ps
tDH(base) DC100	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	45	-	Ps
Data Strobe Timing				
Symbol	Parameter	Min.	Max.	Unit
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	Parameter	Min.	Max.	Unit
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nC K, 7.5ns)	-	

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tWTR	Delay from start of internal write transaction to Internal read command	max(4nC K, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12n CK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 *tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nC K, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nC K, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
1.35V				
tIS(base) AC160	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	60	-	Ps
tIS(base) AC135		185	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	130	-	Ps
1.5V				
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	45	-	Ps
tIS(base) AC150		170	-	Ps
tIS(base) AC135		-	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	120	-	Ps
Calibration Timing				
Symbol	Parameter	Min.	Max.	Unit
tZQinit	Power-up and RESET calibration time	512	-	nCK

Specifications subject to change without notice, contact your sales representatives for the most update information.

tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC + 10ns)	-	
Self Refresh Timings				
Symbol	Parameter	Min.	Max.	Unit
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC+10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min)+1tCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, 10ns)	-	
Power Down Timings				
Symbol	Parameter	Min.	Max.	Unit
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK

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tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	Parameter	Min.	Max.	Unit
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	Parameter	Min.	Max.	Unit
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	165	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	165	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

9. SERIAL PRESENCE DETECT SPECIFICATION

Byte	Description	Function Supported	Serial PD Data Entry (Hexadecimal)
0	Number of Serial PD Bytes Written during Production	112/256/176 Bytes	92
1	SPD Revision	SPD Revision 1.3	13
2	Key Byte/DRAM Device Type	DDR3-DRAM	0B
3	Key Byte/Module type	SODIMM	03
4	SDRAM Density and Banks	8 Banks, 4Gb	04
5	SDRAM Address	16/10	21
6	Reserve	1.35V Operable	02
7	Module Organization	2 Rank x8	09
8	Module Memory Bus Width	64bit Bus	03
9	Fine Timebase (FTB) Dividend/Divisor	DDR3-Fine Timebase Dividend/Divisor	11
10	Medium Timebase (MTB) Dividend	1	01
11	Medium Timebase (MTB) Divisor	8	08
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3-Min SDRAM Cycle Time	0A
13	Reserve	Reserved	00
14	CAS latency, least Significant Byte	DDR3-CAS LATENCIES SUPPORTED	FE
15	CAS latency, most Significant Byte	DDR3-CAS LATENCIES SUPPORTED	00
16	Minimum CAS Latency Time (tAamin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	DDR3-MIN ROW ACTIVE TO ROW ACTIVE DELAY	30
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69
21	Upper Nibbles for tRAS and tRC	Refer to Byte 22,23	11
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	35ns	18
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	48.125ns	81

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24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260ns	20
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260ns	08
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	Refer Byte 29	00
29	Minimum Four Activate Window Delay Time (tFAWmin)	DDR3-MIN FOUR ACTIVE WINDOW DELAY	F0
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	DDR3-SDRAM DEVICE THERMAL REFRESH OPTIONS	05
32	Module Thermal Sensor	Thermal Sensor	80
33	SDRAM Device Type	Mono-Die	00
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	1.071ns	00
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	13.125ns	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	00
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.125ns	00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	47.125ns	00
39-40	Reserve	Reserve	00
41	SDRAM Maximum Activate Count (MAC) Value		88
42-59	Reserve	Reserve	00
60-63	Module Type Specific Section,	-	0F 11 41 00
64-116	Reserve	-	00
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Advantech	8A C8
119	Module ID: Module Manufacturing Location	-	02
120-121	Module ID: Module Manufacturing Date	-	-
122-125	Module Serial Number	-	-
126-127	SPD Cyclical Redundancy Code	-	3A E0
128-145	Module Part Number	SQR-SD3N8G1K6MNEPB	53 51 52 2D 53 44 33 4E 38 47 31 4B 36 4D 4E 45 50 42

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146-147	Module Revision Code	-	00 00
148-149	DRAM Module Manufacturer's JEDEC ID Code	Micron	80 2C
150-175	Manufacturer's Specific Data	-	-
176-255	Open for customer use	-	-

Appendix: Part Number Table

Product	Advantech PN
SGRAM 8G SO-DDR3L-1600 0~85, Micron	SQR-SD3N8G1K6MNEPB