

UDIMM DDR3L 1600 8GB

Datasheet

(SQR-UD3N-8G1K6SNEB)

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Revision History

Rev	Date	Modification
1.0	13 th Jul., 2019	Official released.

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1. Features

● Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-12800	P	1066	1333	1600	13.125	13.125	13.125

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- CL-tRCD-tRP: 11-11-11
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (-0.067V/+0.1V) or 1.5Volt (-0.1V/+0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- On-Board thermal sensor (Class B)
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (TA ≤ +85°C)
- 15/10/1 Addressing (row/column/rank)-8GB
- Golden Connector (Au: 30μ")
- SDRAM operating temperature range 0°C ≤ TCASE ≤ +85°C
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 7, 9, 11
 - Burst Length: switch on-the-fly: BL=8 or BC 4

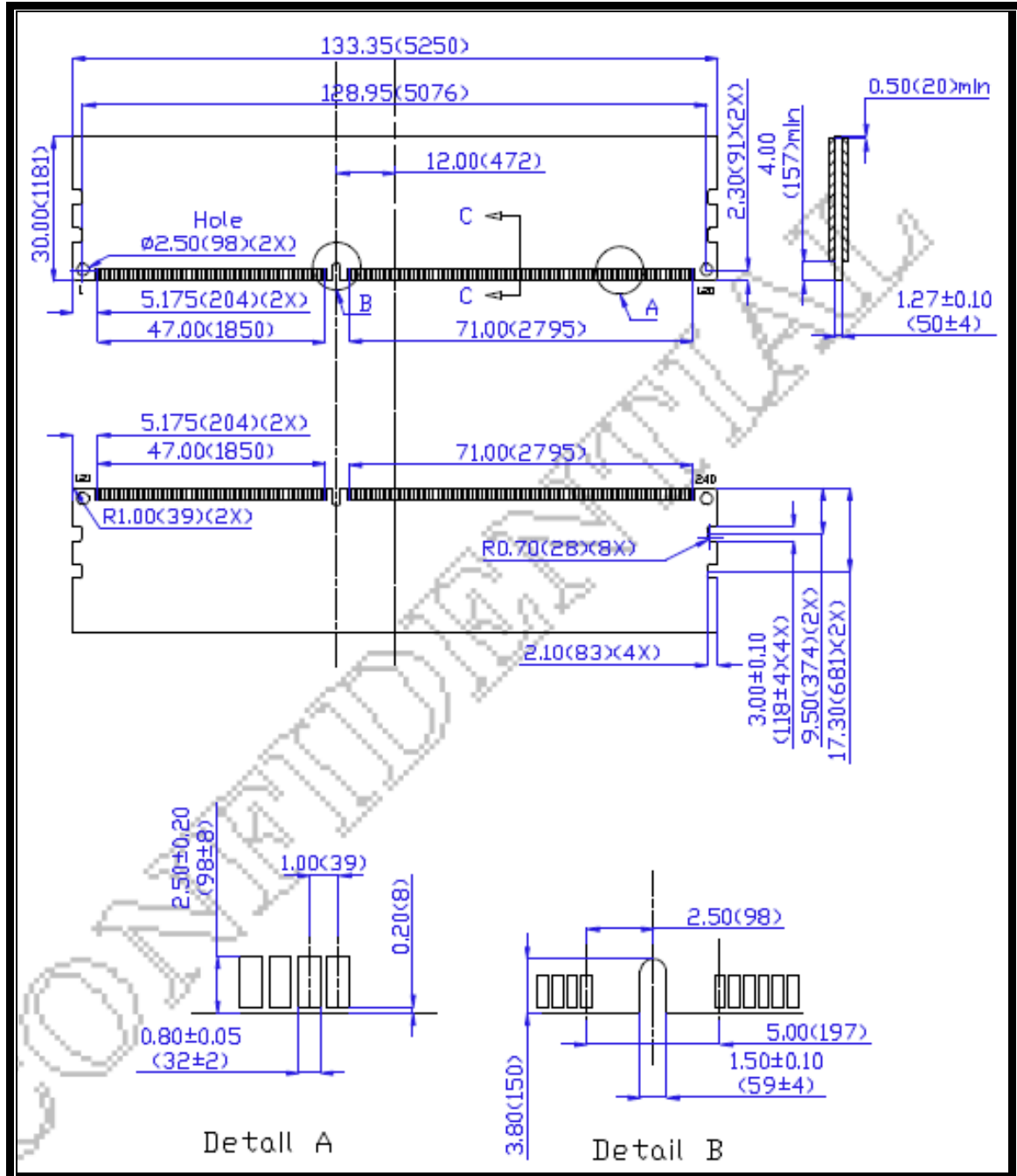
2. Order Information

Extend Temperature DDR3L UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	Thermal Sensor
SQR-UD3N-8G1K6SNEB	8GB	PC3-12800	1024Mx64	16	2	Y

- SDRAM TCASE: 0°C~85°C
- SDRAM Information: Samsung 512Mx8 E-die

3. Dimension

(8GB, 2 Ranks 512Mx8 DDR3L base UDIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15 (6), unless otherwise specified.

4. Pin Identification

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I ² C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I ² C serial bus data line for EEPROM
/RAS	SDRAM row address strobe	SA0-SA2	I ² C slave address select for EEPROM
/CAS	SDRAM column address strobe	VDD	SDRAM core power supply
/WE	SDRAM write enable	VDDQ	SDRAM I/O Driver power supply
/S0-/S1	DIMM Rank Select Lines	VREFDQ	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	VSS	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	VDDSPD	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits (for x72 module)	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
/DQS0–/DQS8	SDRAM data strobes (negative line of differential pair)	/RESET	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	/EVENT	Reserved for optional temperature-sensing hardware
CK0–CK1	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
/CK0–/CK1	SDRAM clocks (negative line of differential pair)	RSVD	Reserved for future use

5. Pin Configurations

X64 UDIMM

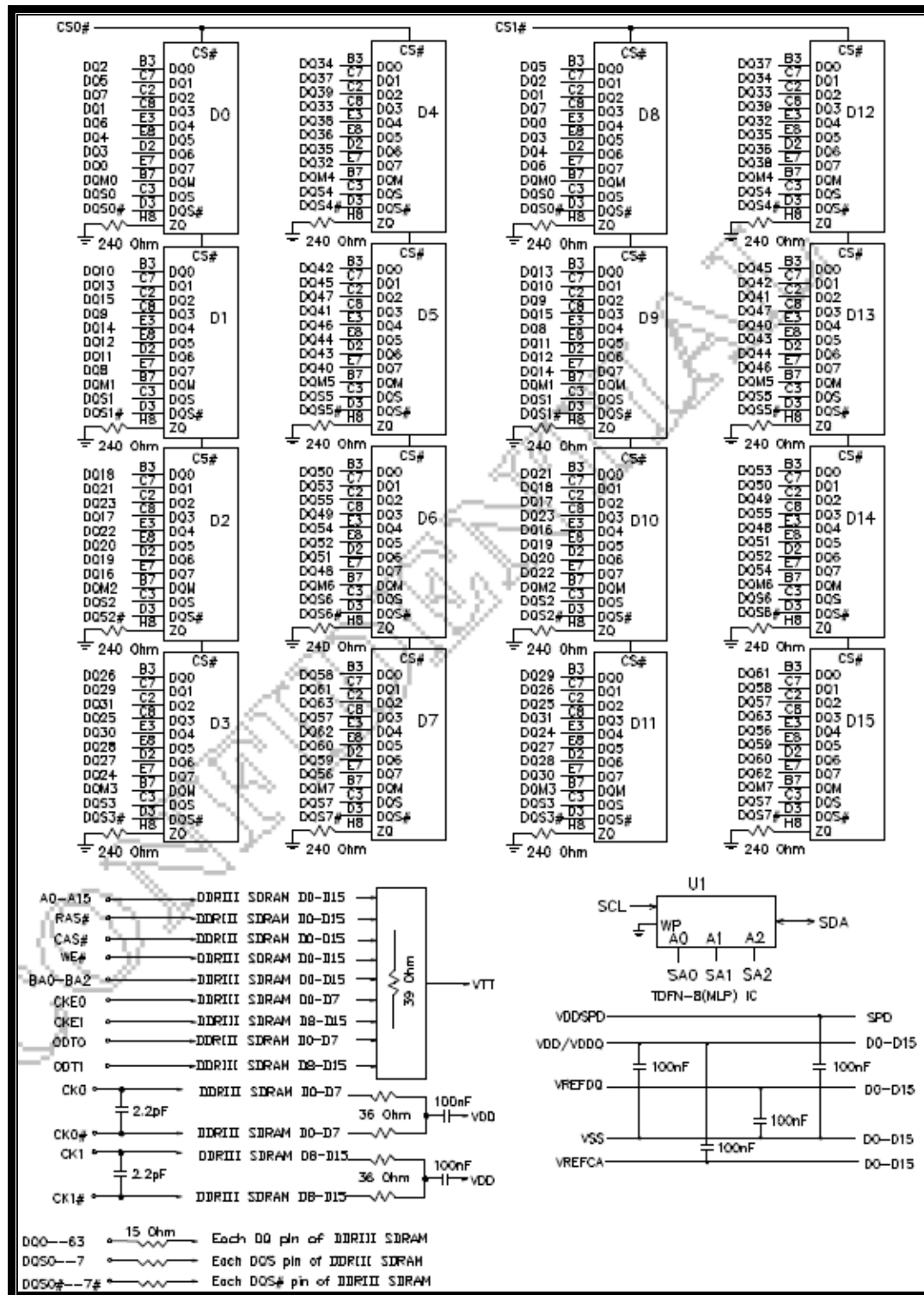
Front								Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3	182	VDD	212	DM5
3	DQ0	33	/DQS3	63	NC,CK1	93	/DQS5	123	DQ5	153	NC	183	VDD	213	NC
4	DQ1	34	DQS3	64	NC,CK1	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	NC	98	VSS	128	DQ6	158	NC	188	A0	218	DQ52
9	DQ2	39	NC	69	VDD	99	DQ48	129	DQ7	159	NC	189	VDD	219	DQ53
10	DQ3	40	NC	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	NC	191	VDD	221	DM6
12	DQ8	42	NC	72	VDD	102	/DQS6	132	DQ13	162	NC	192	/RAS	222	NC
13	DQ9	43	NC	73	/WE	103	DQS6	133	VSS	163	VSS	193	/S0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1	164	NC	194	VDD	224	DQ54
15	/DQS1	45	NC	75	VDD	105	DQS0	135	NC	165	NC	195	ODT0	225	DQ55
16	DQS1	46	NC	76	/S1, NC	106	DQS1	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1, NC	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	NC	78	VDD	108	DQS6	138	DQ15	168	/RESET	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQS7	139	VSS	169	CKE1, NC	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	NC	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQS8	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQS9	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

1. Pin76, 77, 169: /S1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs

2. Pin63, 64: CK1, /CK1 Used for dual-rank UDIMMs; not used on single-rank DIMMs

6. Block Diagram

(8GB, 2 Ranks 512Mx8 DDR3L SDRAMs)



7. Environmental Requirements

DDR3 UDIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +85	°C	3
TSTG	Storage Temperature	-50 to +100	°C	1
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2
Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Note 2 Up to 9850 ft. Note 3 The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR3 DRAM component specification. Following JEDEC specifications.				

8. SDRAM Parameters by device density

RTT_Nom Setting	Parameter	4Gb	Units
tRFC	REF command ACT or REF command time	260	ns
tREFI	Average periodic refresh interval	0°C ≤ TCASE ≤ 85°C	7.8
		85°C ≤ TCASE ≤ 95°C	3.9

9. Parameter & Operating Conditions

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.80	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.80	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.80	V	4,6

Note:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

AC & DC Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
Recommended DC Operating Conditions - DDR3L (1.35V) operation						
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
VDDQ	Supply Voltage	1.283	1.35	1.45	V	1,2
Recommended DC Operating Conditions - DDR3 (1.5V) operation						
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
VDDQ	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
VIH (DC) DDR3L	DC Input High (Logic1) Voltage	VREF + 90	-	VDD	V	3
VIH (DC) DDR3	DC Input High (Logic1) Voltage	VREF + 100		VDD	V	3
VIL (DC) DDR3L	DC Input Low (Logic 0) Voltage	VSS	-	VREF - 90	V	3
VIL (DC) DDR3	DC Input Low (Logic 0) Voltage	VSS		VREF - 100	V	3
VIH (AC) DDR3L	AC Input High (Logic1) Voltage	VREF+ 135	-	-	V	3
VIH (AC) DDR3	AC Input High (Logic1) Voltage	VREF+ 150			V	3
VIL (AC) DDR3L	AC Input Low (Logic 0) Voltage	-	-	VREF - 135	V	3
VIL (AC) DDR3	AC Input Low (Logic 0) Voltage			VREF - 150	V	3
VREFDQ (DC)	Reference Voltage for DQ, DM inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5
VREFCA (DC)	Reference Voltage for ADD,CMD inputs	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4,5

Single Ended AC/DC Output Levels						
VOH (DC)	DC output high measurement level (for IV curve linearity)	-	$0.8 \times VDDQ$	-	V	
VOM (DC)	DC output mid measurement level (for IV curve linearity)	-	$0.5 \times VDDQ$	-	V	
VOL (DC)	DC output low measurement level (for IV curve linearity)	-	$0.2 \times VDDQ$	-	V	
VOH (AC)	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times VDDQ$	-	V	6
VOL (AC)	AC output low measurement level (for output SR)		$V_{TT} - 0.1 \times VDDQ$	-	V	6
Differential AC/DC Input Levels						
VIHdiff DDR3L	Differential Input high	+0.18	-	Note 9	V	7
VIHdiff DDR3	Differential Input high	+0.2		Note 9	V	7
VILdiff DDR3L	Differential Input logic Low	Note 9	-	-0.18	V	7
VILdiff DDR3	Differential Input logic Low	Note 9	-	-0.2	V	7
VIHdiff(ac) DDR3L	Differential Input high ac	$2 * (V_{IH} (AC) - V_{REF})$	-	Note 9	V	8
VIHdiff(ac) DDR3	Differential Input high ac	$2 * (V_{IH} (AC) - V_{REF})$	-	Note 9	V	8
VILdiff(ac) DDR3L	Differential Input logic Low ac	Note 9	-	$2 * (V_{REF} - V_{IL} (AC))$	V	8
VILdiff(ac) DDR3	Differential Input logic Low ac	Note 9	-	$2 * (V_{REF} - V_{IL} (AC))$	V	8
Differential AC and DC Output Levels						
VOHdiff(AC)	AC differential output high measurement level (for output SR)	-	$+ 0.2 \times VDDQ$	-	V	10
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-	$- 0.2 \times VDDQ$	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA.
4. Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV)
5. For reference: approx. VDD/2.
6. The swing of $\pm 0.1 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = VDDQ/2$
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of $\pm 0.2 \times VDDQ$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = VDDQ/2$ at each of the differential outputs.

Operating, Standby, and Refresh Currents

- 8GB UDIMM (1 Rank, 512Mx8 DDR3L SDRAMs TCASE = 0 °C ~ 85 °C)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active - Precharge		416	mA
I DD1	One bank; Active - Read - Precharge		576	mA
I DD2N	Precharge Standby Current		176	mA
IDD2NT	Precharge Standby ODT Current		208	mA
I DD2P	Precharge Power Down Current	Fast Mode	128	mA
	Precharge Power Down Current	Slow Mode	128	mA
I DD2Q	Precharge Quiet Standby Current		160	mA
I DD3N	Active Standby Current		336	mA
I DD3P	Active Power-Down Current		160	mA
I DD4R	Operating Current Burst Read		1024	mA
I DD4W	Operating Current Burst Write		1008	mA
I DD5B	Burst Refresh Current		3040	mA
I DD6	Self-Refresh Current: Normal Temperature Range		192	mA
I DD7	Operating Bank Interleave Read Current		1936	mA
I DD8	RESET Low Current		240	mA

Timing Parameters & Specifications

(TCASE = 0 °C ~ 85 °C; VDDQ = VDD , See AC Characteristics)

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.25	<1.5	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps
TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	Parameter	Min.	Max.	Unit
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
1.35V				
tDS(base) AC160	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC135		25	-	Ps
tDS(base)		-	-	Ps

AC125				
tDH(base) DC90	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	55	-	Ps
1.5V				
tDS(base) AC175	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC150		10	-	Ps
tDS(base) AC135		-	-	Ps
tDH(base) DC100	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	45	-	Ps
Data Strobe Timing				
Symbol	Parameter	Min.	Max.	Unit
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	Parameter	Min.	Max.	Unit
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 *tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nC K, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nC K, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
1.35V				
tIS(base) AC160	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	60	-	Ps
tIS(base) AC135		185	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	130	-	Ps
1.5V				
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	45	-	Ps
tIS(base) AC150		170	-	Ps
tIS(base) AC135		-	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	120	-	Ps
Calibration Timing				
Symbol	Parameter	Min.	Max.	Unit
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nC K, tRFC + 10ns)	-	
Self Refresh Timings				
Symbol	Parameter	Min.	Max.	Unit
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC+10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min)+1tCK	-	

tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	Parameter	Min.	Max.	Unit
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	Parameter	Min.	Max.	Unit
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps

tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	Parameter	Min.	Max.	Unit
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	165	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	165	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

SERIAL PRESENCE DETECT SPECIFICATION

2 RANK UDIMM DIMM based on 512Mx8, 8Banks, 8K Refresh, DDR3L SDRAMs with SPD

Byte	Description	Function Supported	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	112/256/176 Bytes	92	
1	SPD Revision	SPD Revision 1.2	13	
2	Key Byte/DRAM Device Type	DDR3-DRAM	0B	
3	Key Byte/Module type	UDIMM	02	
4	SDRAM Density and Banks	8 Banks, 4Gb	04	
5	SDRAM Address	16/10	21	
6	Reserve	1.35V Operable	02	
7	Module Organization	2 Rank x8	09	
8	Module Memory Bus Width	64bit Bus	03	
9	Fine Timebase (FTB) Dividend/Divisor	DDR3-Fine Timebase Dividend/Divisor	11	
10	Medium Timebase (MTB) Dividend	1ns	01	
11	Medium Timebase (MTB) Divisor	8	08	
12	SDRAM Minimum Cycle Time (tCKmin)	DDR3-Min SDRAM Cycle Time	0A	
13	Reserve	Reserved	00	
14	CAS latency, least Significant Byte	DDR3-CAS LATENCIES SUPPORTED	FC	
15	CAS latency, most Significant Byte	DDR3-CAS LATENCIES SUPPORTED	00	
16	Minimum CAS Latency Time (tAamin)	13.125ns	69	
17	Minimum Write Recovery Time (tWRmin)	15ns	78	
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	69	
19	Minimum Row Active to Row Active	DDR3-MIN ROW ACTIVE TO	30	

	Delay Time (tRRDmin)	ROW ACTIVE DELAY		
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69	
21	Upper Nibbles for tRAS and tRC	Refer to Byte 22,23	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	35ns	18	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	48.125ns	81	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	260ns	20	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	260ns	08	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C	
28	Upper Nibble for tFAW	Refer Byte 29	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	DDR3-MIN FOUR ACTIVE WINDOW DELAY	F0	
30	SDRAM Optional Features	DLL Off, RZQ/6, RZQ/7	83	
31	SDRAM Thermal and Refresh Options	DDR3-SDRAM DEVICE THERMAL REFRESH OPTIONS	01	
32	Module Thermal Sensor	Thermal Sensor	00	
33	SDRAM Device Type	Mono-Die	00	
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	1.071ns	00	
35	Fine Offset for Minimum CAS Latency Time (tAamin)	13.125ns	00	
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	00	
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.125ns	00	
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	47.125ns	00	
39-40	Reserve	Reserve	00	

41	SDRAM Maximum Activate Count (MAC) Value		88	
42-59	Reserve	Reserve	00	
60-63	Module Type Specific Section,	-	0F 11 21 01	
64-116	Reserve	-	00	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Advantech	8A C8	
119	Module ID: Module Manufacturing Location	-	02	
120-121	Module ID: Module Manufacturing Date	-	-	
122-125	Module Serial Number	-	-	
126-127	SPD Cyclical Redundancy Code	-	73 F0	
128-145	Module Part Number	SQR-UD3N-8G1K6SNEB	53 51 52 2D 55 44 33 4D 2D 38 47 31 4B 36 53 4E 4C 42	
146-147	Module Revision Code	-	00 00	
148-149	DRAM Module Manufacturer's JEDEC ID Code	-		
150-175	Manufacturer's Specific Data	-	-	
176-255	Open for customer use	-	-	

Appendix: Part Number Table

Product	Advantech PN
SGRAM 8G U-DDR3L-1600 512x8 SAM (0~85°C)	SQR-UD3N-8G1K6SNEB