

# **UDIMM DDR5 4800 8GB**

## **Datasheet**

**(SQR-UD5N16G4K8MNAB)**

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## Revision History

| Rev | Date                       | Modification     |
|-----|----------------------------|------------------|
| 1.0 | 1 <sup>st</sup> May., 2022 | Offiicla release |

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## 1. Description

| DDR5 UDIMM                                              |         |           |                   |                |                |      |     |
|---------------------------------------------------------|---------|-----------|-------------------|----------------|----------------|------|-----|
| Part Number                                             | Density | Data rate | DIMM Organization | Number of DRAM | Number of rank | side | ECC |
| <b>SQR-UD5N16G4K8MNAB</b><br>(Micron 1Gx16(16Gb) A-die) | 8GB     | 4800 MT/s | 1Gx64             | 4              | 1              | 1    | N   |

## 2. Features

### ● Key Parameter

| Data transfer rate | tCK (ns) | tRCD (ns) | tRP (ns) | tRAS (ns) | tRC (ns) |
|--------------------|----------|-----------|----------|-----------|----------|
| 4800 MT/s          | 0.416    | 16.00     | 16.00    | 32        | 48.00    |

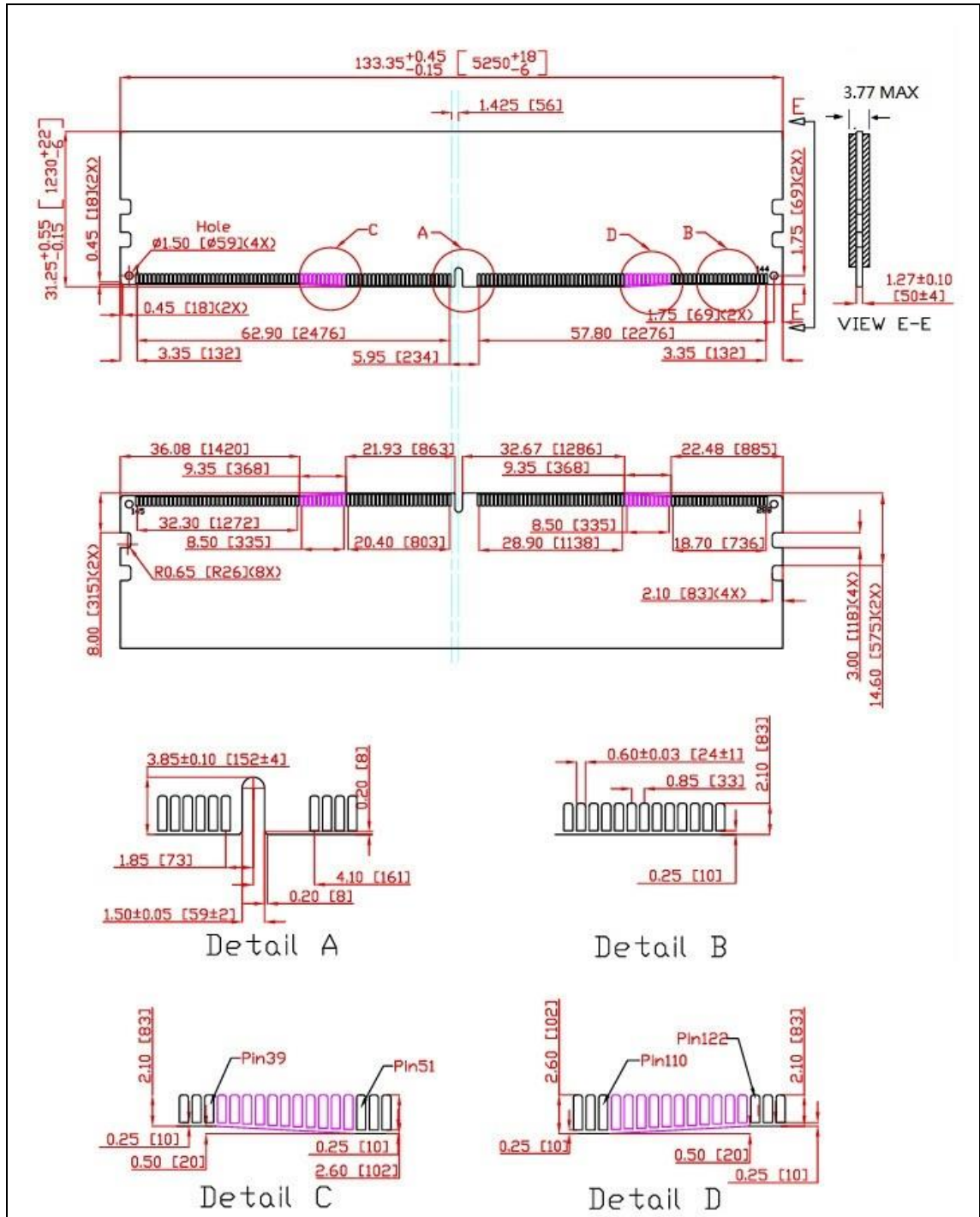
### ● tRFC parameter by Density

| Parameter  | 8Gb | 16Gb | 24Gb | 32Gb | Unit |
|------------|-----|------|------|------|------|
| tRFC1,min  | 195 | 295  | TBD  | TBD  | ns   |
| tRFC2,min  | 130 | 160  | TBD  | TBD  | ns   |
| tRFCsb,min | 115 | 130  | TBD  | TBD  | ns   |

- JEDEC Standard 288-pin Dual In-Line Memory Module
- Cl-tRCD-tRP: 40-39-39
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42
- Operating temperature Tcase: 0-95°C
  - ◆ tREFI 3.9us for 0°C ≤ Tcase < 85°C
  - ◆ tREFI 1.95us for 85°C < Tcase ≤ 95°C
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

## 3. Dimension

- (8GB, 1Rank 1Gx16 DDR5 base UDIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of  $\pm 0.15$  (6), unless otherwise specified.

## 4. Pin Descriptions

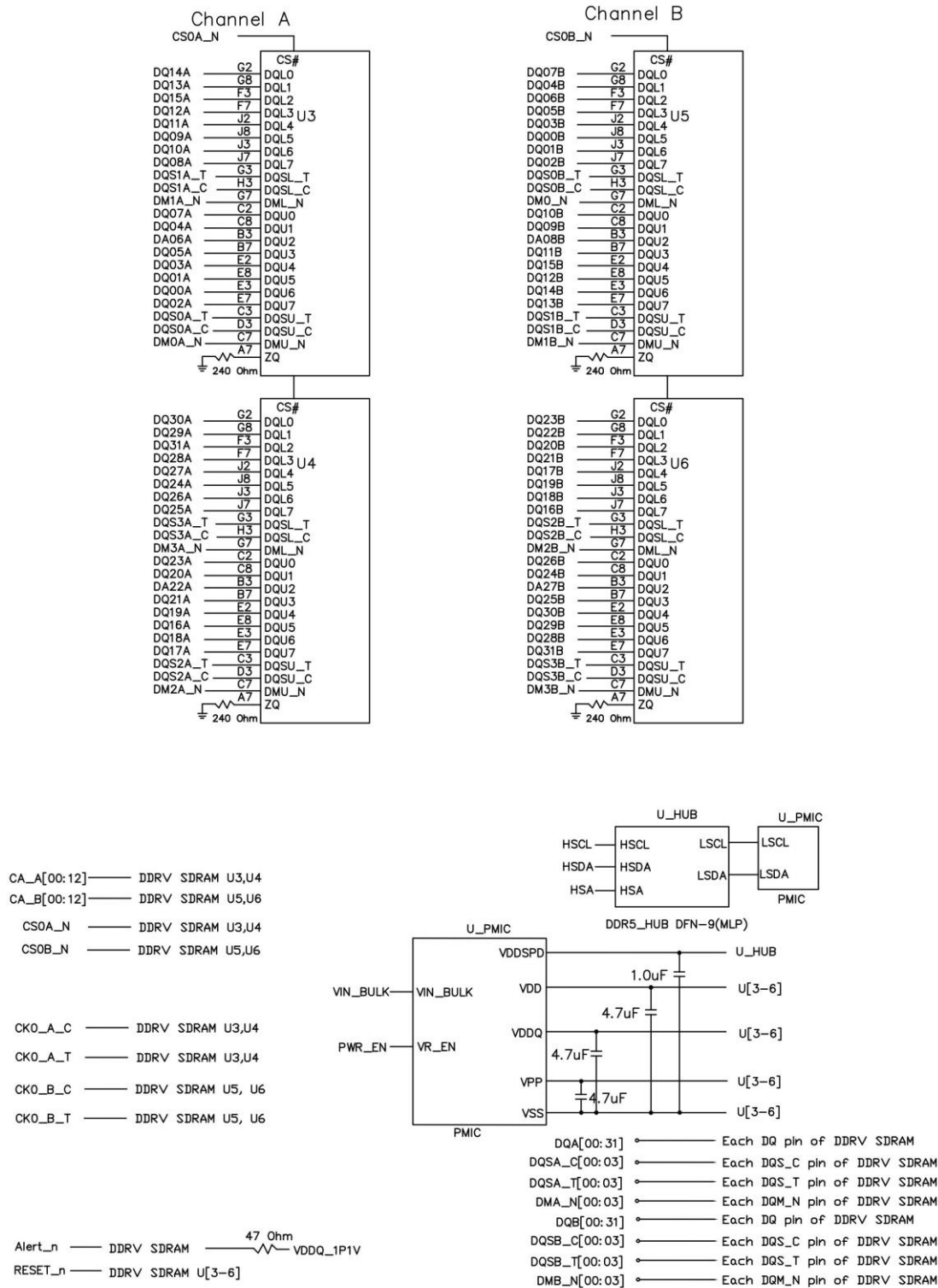
| Symbol                   | Type             | I/O Level | Description                   | Symbol                       | Type             | I/O Level | Description                 |
|--------------------------|------------------|-----------|-------------------------------|------------------------------|------------------|-----------|-----------------------------|
| CK_t, CK_c               | Input            | VDDQ      | Clock:                        | DQ[31:0]_A<br>DQ[31:0]_B     | Input/<br>Output | VDDQ      | Data Input/Output           |
| CA[12:0]_A<br>CA[12:0]_B | Input            | VDDQ      | Command/Address Inputs        | CB[3:0]_A<br>CB[3:0]_B       | Input/<br>Output | VDDQ      | ECC Check Bits Input/Output |
| CS[1:0]_A<br>CS[1:0]_B   | Input            | VDDQ      | Chip Select                   | DQS[4:0]_A_t<br>DQS[4:0]_B_t | Input/<br>Output | VDDQ      | Data Strobe                 |
| ALERT_n                  | Output           | VDDQ      | Alert                         | DQS[4:0]_A_c<br>DQS[4:0]_B_c | Input/<br>Output | VDDQ      | Data Strobe                 |
| RESET_n                  | CMOS<br>Input    | VDDQ      | Active Low Asynchronous Reset | DM[3:0]_A_n<br>DM[3:0]_B_n   | Input            | VDDQ      | Input Data Mask             |
| PWR_GOOD                 | Input/<br>Output | VDDQ      | Power Good Indicator          | VIN_BULK                     | Supply           |           | External Power Supply       |
| HSCL                     | Input            | VOUT      | Host Sideband Bus Clock       | PWR_EN                       | Input            |           | PMIC Enable                 |
| HSDA                     | Input/<br>Output | VOUT      | Host Sideband Bus Data        | VSS                          | Supply           |           | Ground                      |
| HAS                      | Input            | GND       | Host Sideband Bus Device ID   | RFU                          |                  |           | Reserved for future use     |

## 5. Pin Assignments

DDR5 1Gx16 base UDIMM

| 288-Pin DDR5 UDIMM Front |          |     |          |     |          |     |          | 288-Pin DDR5 UDIMM Back |          |     |          |     |          |     |          |
|--------------------------|----------|-----|----------|-----|----------|-----|----------|-------------------------|----------|-----|----------|-----|----------|-----|----------|
| Pin                      | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin                     | Symbol   | Pin | Symbol   | Pin | Symbol   | Pin | Symbol   |
| 1                        | VIN_BULK | 37  | DQ20_A   | 73  | CK0_A_c  | 109 | Vss      | 145                     | VIN_BULK | 181 | DQ22_A   | 217 | CK1_A_c  | 253 | Vss      |
| 2                        | RFU      | 38  | Vss      | 74  | Vss      | 110 | DQ5_B    | 146                     | VIN_BULK | 182 | Vss      | 218 | Vss      | 254 | DQ7_B    |
| 3                        | RFU      | 39  | DQ21_A   | 75  | RFU      | 111 | Vss      | 147                     | PWR_GOOD | 183 | DQ23_A   | 219 | RFU      | 255 | Vss      |
| 4                        | HSDL     | 40  | Vss      | 76  | RFU      | 112 | DQ8_B    | 148                     | HAS      | 184 | Vss      | 220 | RFU      | 256 | DQ10_B   |
| 5                        | HSDA     | 41  | DQ24_A   | 77  | Vss      | 113 | Vss      | 149                     | RFU      | 185 | DQ26_A   | 221 | Vss      | 257 | Vss      |
| 6                        | Vss      | 42  | Vss      | 78  | CK0_B_t  | 114 | DQ9_B    | 150                     | Vss      | 186 | Vss      | 222 | CK1_B_t  | 258 | DQ11_B   |
| 7                        | RFU      | 43  | DQ25_A   | 79  | CK0_B_c  | 115 | Vss      | 151                     | PWR_EN   | 187 | DQ27_A   | 223 | CK1_B_c  | 259 | Vss      |
| 8                        | Vss      | 44  | Vss      | 80  | Vss      | 116 | DM1_B_n  | 152                     | RFU      | 188 | Vss      | 224 | Vss      | 260 | DQS1_B_c |
| 9                        | DQ0_A    | 45  | DM3_A_n  | 81  | RFU      | 117 | Vss      | 153                     | Vss      | 189 | DQS3_A_c | 225 | RFU      | 261 | DQS1_B_t |
| 10                       | Vss      | 46  | Vss      | 82  | CA12_B   | 118 | DQ12_B   | 154                     | DQ2_A    | 190 | DQS3_A_t | 226 | RFU      | 262 | Vss      |
| 11                       | DQ1_A    | 47  | DQ28_A   | 83  | Vss      | 119 | Vss      | 155                     | Vss      | 191 | Vss      | 227 | Vss      | 263 | DQ14_B   |
| 12                       | Vss      | 48  | Vss      | 84  | CA10_B   | 120 | DQ13_B   | 156                     | DQ3_A    | 192 | DQ30_A   | 228 | CA11_B   | 264 | Vss      |
| 13                       | DQ0_A_c  | 49  | DQ29_A   | 85  | CA8_B    | 121 | Vss      | 157                     | Vss      | 193 | Vss      | 229 | CA9_B    | 265 | DQ15_B   |
| 14                       | DQS0_A_t | 50  | Vss      | 86  | Vss      | 122 | DQ16_B   | 158                     | DM0_A_n  | 194 | DQ31_A   | 230 | Vss      | 266 | Vss      |
| 15                       | Vss      | 51  | CB0_A    | 87  | CA6_B    | 123 | Vss      | 159                     | Vss      | 195 | Vss      | 231 | CA7_B    | 267 | DQ18_B   |
| 16                       | DQ4_A    | 52  | Vss      | 88  | CA4_B    | 124 | DQ17_B   | 160                     | DQ6_A    | 196 | CB2_A    | 232 | CA5_B    | 268 | Vss      |
| 17                       | Vss      | 53  | CB1_A    | 89  | Vss      | 125 | Vss      | 161                     | Vss      | 197 | Vss      | 233 | Vss      | 269 | DQ19_B   |
| 18                       | DQ5_A    | 54  | Vss      | 90  | CA2_B    | 126 | DQS2_B_c | 162                     | DQ7_A    | 198 | CB3_A    | 234 | CA3_B    | 270 | Vss      |
| 19                       | Vss      | 55  | DQS4_A_c | 91  | CA0_B    | 127 | DQS2_B_t | 163                     | Vss      | 199 | Vss      | 235 | CA1_B    | 271 | DM2_B_n  |
| 20                       | DQ8_A    | 56  | DQS4_A_t | 92  | Vss      | 128 | Vss      | 164                     | DQ10_A   | 200 | ALERT_n  | 236 | Vss      | 272 | Vss      |
| 21                       | Vss      | 57  | Vss      | 93  | CS0_B_n  | 129 | DQ20_B   | 165                     | Vss      | 201 | Vss      | 237 | CS1_B_n  | 273 | DQ22_B   |
| 22                       | DQ9_A    | 58  | CS0_A_n  | 94  | Vss      | 130 | Vss      | 166                     | DQ11_A   | 202 | CS1_A_n  | 238 | Vss      | 274 | Vss      |
| 23                       | Vss      | 59  | Vss      | 95  | RESET_n  | 131 | DQ21_B   | 167                     | Vss      | 203 | Vss      | 239 | DQS4_B_c | 275 | DQ23_B   |
| 24                       | DM1_A_n  | 60  | CA0_A    | 96  | Vss      | 132 | Vss      | 168                     | DQS1_A_c | 204 | CA1_A    | 240 | DQS4_B_t | 276 | Vss      |
| 25                       | Vss      | 61  | CA2_A    | 97  | CB0_B    | 133 | DQ24_B   | 169                     | DQS1_A_t | 205 | CA3_A    | 241 | Vss      | 277 | DQ26_B   |
| 26                       | DQ12_A   | 62  | Vss      | 98  | Vss      | 134 | Vss      | 170                     | Vss      | 206 | Vss      | 242 | CB2_B    | 278 | Vss      |
| 27                       | Vss      | 63  | CA4_A    | 99  | CB1_B    | 135 | DQ25_B   | 171                     | DQ14_A   | 207 | CA5_A    | 243 | Vss      | 279 | DQ27_B   |
| 28                       | DQ13_A   | 64  | CA6_A    | 100 | Vss      | 136 | Vss      | 172                     | Vss      | 208 | CA7_A    | 244 | CB3_B    | 280 | Vss      |
| 29                       | Vss      | 65  | Vss      | 101 | DQ0_B    | 137 | DM3_B_n  | 173                     | DQ15_A   | 209 | Vss      | 245 | Vss      | 281 | DQS3_B_c |
| 30                       | DQ16_A   | 66  | CA8_A    | 102 | Vss      | 138 | Vss      | 174                     | Vss      | 210 | CA9_A    | 246 | DQ2_B    | 282 | DQS3_B_t |
| 31                       | Vss      | 67  | CA10_A   | 103 | DQ1_B    | 139 | DQ28_B   | 175                     | DQ18_A   | 211 | CA11_A   | 247 | Vss      | 283 | Vss      |
| 32                       | DQ17_A   | 68  | Vss      | 104 | Vss      | 140 | Vss      | 176                     | Vss      | 212 | Vss      | 248 | DQ3_B    | 284 | DQ30_b   |
| 33                       | Vss      | 69  | CA12_A   | 105 | DQS0_B_c | 141 | DQ29_B   | 177                     | DQ19_A   | 213 | RFU      | 249 | Vss      | 285 | Vss      |
| 34                       | DQS2_A_c | 70  | RFU      | 106 | DQS0_B_t | 142 | Vss      | 178                     | Vss      | 214 | RFU      | 250 | DM0_B_n  | 286 | DQ31_B   |
| 35                       | DQS2_A_t | 71  | Vss      | 107 | Vss      | 143 | RFU      | 179                     | DM2_A_n  | 215 | Vss      | 251 | Vss      | 287 | Vss      |
| 36                       | Vss      | 72  | CK0_A_t  | 108 | DQ4_B    | 144 | RFU      | 180                     | Vss      | 216 | CK1_A_t  | 252 | DQ6_B    | 288 | RFU      |

## 6. Block Diagram



## 7. Thermal Characteristics

| Symbol           | Parameter                                                |                        | Rating     | Units | Note    |
|------------------|----------------------------------------------------------|------------------------|------------|-------|---------|
| T <sub>c</sub>   | Operation Temperature                                    | Normal Operating Temp. | 0 to 85    | °C    | 1,2,3   |
|                  |                                                          | Extended Temp.         | 85 to 95   | °C    | 1,2,3,4 |
| T <sub>STG</sub> | Storage Temperature                                      |                        | -55 to 100 | °C    | 5       |
| HSTG             | Non-operating storage relative humidity (non-condensing) |                        | 5 to 95    | %     |         |

**Note:**

1. Maximum operating case temperature; T<sub>c</sub> is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T<sub>c</sub> during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T<sub>c</sub> during operation.
4. If T<sub>c</sub> exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

## 8. IDD, IDDQ and IPP Specifications

| Symbol | Description                                      | Value<br>(Typical) |          | Units |
|--------|--------------------------------------------------|--------------------|----------|-------|
|        |                                                  | IDD Max.           | IPP Max. |       |
| IDD0   | Operating One Bank Active-Precharge Current      | 488                | 40       | mA    |
| IDD0F  | Operating Four Bank Active-Precharge Current     | 656                | 52       | mA    |
| IDD2N  | Precharge Standby Current                        | 368                | 24       | mA    |
| IDD2P  | Precharge Power-Down Current                     | 352                | 24       | mA    |
| IDD3N  | Active Standby Current                           | 568                | 28       | mA    |
| IDD3P  | Active Power-Down Current                        | 560                | 28       | mA    |
| IDD4R  | Operating Burst Read Current                     | 2120               | 36       | mA    |
| IDD4W  | Operating Burst Write Current                    | 1916               | 256      | mA    |
| IDD5B  | Burst Refresh Current (Normal Refresh Mode)      | 1108               | 112      | mA    |
| IDD5C  | Burst Refresh Current (Same Bank Refresh Mode)   | 540                | 48       | mA    |
| IDD6   | Self Refresh Current: Normal Temperature Range   | 408                | 60       | mA    |
| IDD6E  | Self Refresh Current: Extended Temperature Range | 3100               | 140      | mA    |
| IDD7   | Operating Bank Interleave Read Current           | 320                | 24       | mA    |
| IDD8   | Maximum Power Saving Deep Power Down Current     | 488                | 40       | mA    |

## 9. Timing Parameters

| Parameter                                                                                        | Symbol     | 4400                  |        | 4800                  |        | 5200                  |        | Unit |
|--------------------------------------------------------------------------------------------------|------------|-----------------------|--------|-----------------------|--------|-----------------------|--------|------|
|                                                                                                  |            | Min                   | Max    | Min                   | Max    | Min                   | Max    |      |
| Clock Timing                                                                                     |            |                       |        |                       |        |                       |        |      |
| Average clock period                                                                             | tCK,AVG    | 0.454                 | <0.500 | 0.416                 | <0.454 | 0.384                 | <0.416 | ns   |
| Command and Address Timing                                                                       |            |                       |        |                       |        |                       |        |      |
| Read to Read command delay for same bank group                                                   | tCCD_L     | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | nCK  |
| WRITE to WRITE command delay for same bank group                                                 | tCCD_L_WR  | 32nCK, 20ns (MAX)     |        | 32nCK, 20ns (MAX)     |        | 32nCK, 20ns (MAX)     |        | nCK  |
| WRITE to WRITE command delay for same bank group, second WRITE not RMW                           | tCCD_L_WR2 | 16nCK, 10ns (MAX)     |        | 16nCK, 10ns (MAX)     |        | 16nCK, 10ns (MAX)     |        | nCK  |
| Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF          | tCCD_S     | 8                     |        | 8                     |        | 8                     |        | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size                     | tRRD_S,2K  | 8                     |        | 8                     |        | 8                     |        | nCK  |
| ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size                     | tRRD_S,1K  | 8                     |        | 8                     |        | 8                     |        | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size                          | tRRD_L,2K  | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | nCK  |
| ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size                          | tRRD_L,1K  | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | 8nCK,5ns (MAX)        |        | nCK  |
| Four activate window for 2KB page size                                                           | tFAW,2K    | 40nCK, 18.160ns (MAX) |        | 40nCK, 16.640ns (MAX) |        | 40nCK, 15.360ns (MAX) |        | ns   |
| Four activate window for 1KB page size                                                           | tFAW,1K    | 32nCK, 14.528ns (MAX) |        | 32nCK, 13.312ns (MAX) |        | 32nCK, 12.288ns (MAX) |        | ns   |
| Delay from start of internal WRITE transaction to internal READ command for different bank group | tWTR_S     | 4nCK, 2.5ns (MAX)     |        | 4nCK, 2.5ns (MAX)     |        | 4nCK, 2.5ns (MAX)     |        | ns   |

|                                                                                                           |                |                    |       |                    |      |                    |     |     |
|-----------------------------------------------------------------------------------------------------------|----------------|--------------------|-------|--------------------|------|--------------------|-----|-----|
| Delay from start of internal WRITE transaction to internal READ command for same bank group               | tWTR_L         | 16nCK, 10ns (MAX)  |       | 16nCK, 10ns (MAX)  |      | 16nCK, 10ns (MAX)  |     | ns  |
| Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank | tWTRA          | tWR-tRTP           |       | tWR-tRTP           |      | tWR-tRTP           |     | ns  |
| Internal READ command to PRECHARGE command delay                                                          | tRTP           | 12nCK, 7.5ns (MAX) |       | 12nCK, 7.5ns (MAX) |      | 12nCK, 7.5ns (MAX) |     | ns  |
| PRECHARGE to PRECHARGE delay                                                                              | tPPD           | 2                  |       | 2                  |      | 2                  |     | nCK |
| WRITE recovery time                                                                                       | tWR            | 29.964             |       | 29.952             |      | 29.952             |     | ns  |
| DLL locking time                                                                                          | tDLLK          | 1280               |       | 1536               |      | 1536               |     | nCK |
| <b>Mode Register Read/Write Timing</b>                                                                    |                |                    |       |                    |      |                    |     |     |
| Mode register READ command period                                                                         | tMRR           | 14ns, 16nCK (MAX)  |       | 14ns, 16nCK (MAX)  |      | 14ns, 16nCK (MAX)  |     |     |
| Mode register READ pattern to mode register READ pattern command spacing                                  | tMRR_p         | 8                  |       | 8                  |      | 8                  |     | nCK |
| Mode register WRITE command period                                                                        | tMRW           | 5ns, 8nCK (MAX)    |       | 5ns, 8nCK (MAX)    |      | 5ns, 8nCK (MAX)    |     |     |
| Mode register SET command delay                                                                           | tMRD           | 14ns, 16nCK (MAX)  |       | 14ns, 16nCK (MAX)  |      | 14ns, 16nCK (MAX)  |     |     |
| DFE mode register WRITE update delay time                                                                 | tDFE           | 80                 |       | 80                 |      | 80                 |     | ns  |
| <b>Data Strobe Timing</b>                                                                                 |                |                    |       |                    |      |                    |     |     |
| DQS_t, DQS_c differential READ preamble                                                                   | tRPRE          | TBD                |       | TBD                |      | TBD                |     | tCK |
| DQS_t, DQS_c differential READ postamble                                                                  | tRPST          | TBD                |       | TBD                |      | TBD                |     | tCK |
| DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c                                    | tDQSCK         | -0.286             | 0.286 | -0.3               | 0.3  | TBD                | TBD | tCK |
| DQS_t, DQS_c rising edge output variance window                                                           | tDQSCKI        |                    | 0.475 |                    | 0.49 |                    | TBD | tCK |
| <b>Data Strobe Timing</b>                                                                                 |                |                    |       |                    |      |                    |     |     |
| 2-tCK WRITE preamble enable window                                                                        | tWPRE_EN_2 tCK | 1.5                |       | 1.5                |      | 1.5                |     | tCK |
| 3-tCK WRITE preamble enable window                                                                        | tWPRE_EN_3 tCK | 2.5                |       | 2.5                |      | 2.5                |     | tCK |
| 4-tCK WRITE preamble                                                                                      | tWPRE_EN_4     | 2.5                |       | 2.5                |      | 2.5                |     | tCK |

|                                                                                                                                  |              |                        |                       |                        |                       |                        |                       |     |
|----------------------------------------------------------------------------------------------------------------------------------|--------------|------------------------|-----------------------|------------------------|-----------------------|------------------------|-----------------------|-----|
| enable window                                                                                                                    | tCK          |                        |                       |                        |                       |                        |                       |     |
| DQS_t, DQS_c differential WRITE postamble                                                                                        | tWPST        | TBD                    |                       | TBD                    |                       | TBD                    |                       | tCK |
| Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge                                                    | tDQSoffset   | -0.5                   | 0.5                   | -0.5                   | 0.5                   | -0.5                   | 0.5                   | tCK |
| Write leveling setup time                                                                                                        | tWLS         | -80                    | 80                    | -80                    | 80                    | -80                    | 80                    | ps  |
| Write leveling hold time                                                                                                         | tWLH         | -80                    | 80                    | -80                    | 80                    | -80                    | 80                    | ps  |
| Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)                  | tDQSD        | -0.25 x tWPRE_E N_ntCK | 0.25 x tWPRE_E N_ntCK | -0.25 x tWPRE_E N_ntCK | 0.25 x tWPRE_E N_ntCK | -0.25 x tWPRE_E N_ntCK | 0.25 x tWPRE_E N_ntCK | tCK |
| Host and system voltage/ temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16) | tDQSS        | -0.25 x tWPRE_EN_ntCK  |                       |                        |                       |                        |                       | tCK |
| MPSM Timing                                                                                                                      |              |                        |                       |                        |                       |                        |                       |     |
| MPSM exit to first valid command delay                                                                                           | tMPSMX       | tMRD                   |                       | tMRD                   |                       | tMRD                   |                       | ns  |
| ZQ Calibration Timing                                                                                                            |              |                        |                       |                        |                       |                        |                       |     |
| ZQ calibration time                                                                                                              | tZQCAL       | 1                      |                       | 1                      |                       | 1                      |                       | μs  |
| ZQ calibration latch time                                                                                                        | tZQLAT       | 30ns, 8nCK (MIN)       |                       | 30ns, 8nCK (MIN)       |                       | 30ns, 8nCK (MIN)       |                       |     |
| Reset Timing                                                                                                                     |              |                        |                       |                        |                       |                        |                       |     |
| RESET_n low time for reset initialization with stable power                                                                      | tPW_RESET    | 1                      |                       | 1                      |                       | 1                      |                       | μs  |
| Time after RESET_n assertion to ODT off                                                                                          | tRST_ADC     |                        | 50                    |                        | 50                    |                        | 50                    | ns  |
| Self Refresh Timing                                                                                                              |              |                        |                       |                        |                       |                        |                       |     |
| Command pass disable delay                                                                                                       | tCPDED       | 5ns,8nCK (MAX)         |                       | 5ns,8nCK (MAX)         |                       | 5ns,8nCK (MAX)         |                       |     |
| Self refresh CS_n low pulse width                                                                                                | tCSL         | 10                     |                       | 10                     |                       | 10                     |                       | ns  |
| Self refresh exit CS_n high pulse width                                                                                          | tCSH_Srexit  | 13                     | 30                    | 13                     | 30                    | 13                     | 30                    | ns  |
| Self refresh exit CS_n low pulse width                                                                                           | tCSL_Srexit  | 3nCK                   | 30ns                  | 3nCK                   | 30ns                  | 3nCK                   | 30ns                  |     |
| Self refresh exit CS_n low pulse width with frequency change                                                                     | tCSL_FreqChg | VREFCA_time            |                       | VREFCA_time            |                       | VREFCA_time            |                       | ns  |
| Valid clock equirement before SRX                                                                                                | tCKSRX       | 3.5ns, 8nCK (MAX)      |                       | 3.5ns, 8nCK (MAX)      |                       | 3.5ns, 8nCK (MAX)      |                       | ns  |

|                                                                     |          |                                           |                                     |                                           |                                     |                                           |                                     |     |
|---------------------------------------------------------------------|----------|-------------------------------------------|-------------------------------------|-------------------------------------------|-------------------------------------|-------------------------------------------|-------------------------------------|-----|
| Valid clock requirement after SRE                                   | tCKLCS   | tCPDED + 1nCK                             |                                     | tCPDED + 1nCK                             |                                     | tCPDED + 1nCK                             |                                     | nCK |
| Self refresh exit CS_n HIGH                                         | tCASRX   | 0                                         |                                     | 0                                         |                                     | 0                                         |                                     | ns  |
| Exit self refresh to commands not requiring a locked DLL            | tXS      | tRFC1                                     |                                     | tRFC1                                     |                                     | tRFC1                                     |                                     | ns  |
| Exit self refresh to commands requiring a locked DLL                | tXS_DLL  | tDLLK                                     |                                     | tDLLK                                     |                                     | tDLLK                                     |                                     | ns  |
| <b>Power-Down Timing</b>                                            |          |                                           |                                     |                                           |                                     |                                           |                                     |     |
| Command pass disable delay                                          | tCPDED   | 5ns, 8nCK (MAX)                           |                                     | 5ns, 8nCK (MAX)                           |                                     | 5ns, 8nCK (MAX)                           |                                     | ns  |
| Power-down time                                                     | tPD      | 7.5ns, 8nCK (MAX)                         | 5*tREFI1 (normal)<br>9*tREFI2 (FGR) | 7.5ns, 8nCK (MAX)                         | 5*tREFI1 (normal)<br>9*tREFI2 (FGR) | 7.5ns, 8nCK (MAX)                         | 5*tREFI1 (normal)<br>9*tREFI2 (FGR) | ns  |
| Exit power-down to next valid command                               | tXP      | 7.5ns, 8nCK (MAX)                         |                                     | 7.5ns, 8nCK (MAX)                         |                                     | 7.5ns, 8nCK (MAX)                         |                                     | ns  |
| Timing of ACT command to POWER DOWN ENTRY command                   | tACTPDEN | 2                                         |                                     | 2                                         |                                     | 2                                         |                                     | nCK |
| Timing of PREAb, PREsb or PREpb command to POWER DOWN ENTRY command | tPRPDEN  | 2                                         |                                     | 2                                         |                                     | 2                                         |                                     | nCK |
| Timing of READ or READ w/ AP command to POWER DOWN ENTRY command    | tRDPDEN  | CL + RBL/2+1                              |                                     | CL + RBL/2+1                              |                                     | CL + RBL/2+1                              |                                     | nCK |
| Timing of WRITE command to POWER DOWN ENTRY command                 | tWRPDEN  | CWL + WBL/ 2+ (tWR/ tCK(avg)) +1          |                                     | CWL + WBL/ 2+ (tWR/ tCK(avg)) +1          |                                     | CWL + WBL/ 2+ (tWR/ tCK(avg)) +1          |                                     | nCK |
| Timing of WRITE w/ AP command to POWER DOWN ENTRY command           | tWRAPDEN | CWL + WBL/ 2+ -0.25 x tWPRES_EN_n tCKWR+1 |                                     | CWL + WBL/ 2+ -0.25 x tWPRES_EN_n tCKWR+1 |                                     | CWL + WBL/ 2+ -0.25 x tWPRES_EN_n tCKWR+1 |                                     | nCK |
| Timing of REFAb or REFsb command to POWER DOWN ENTRY command        | tREFPDEN | 2                                         |                                     | 2                                         |                                     | 2                                         |                                     | nCK |
| Timing of MRR command to POWER DOWN ENTRY command                   | tMRRPDEN | CL+8+1                                    |                                     | CL+8+1                                    |                                     | CL+8+1                                    |                                     | nCK |
| Timing of MRW command to POWER DOWN ENTRY command                   | tMRWPDEN | tMRD (MIN)                                |                                     | tMRD (MIN)                                |                                     | tMRD (MIN)                                |                                     | nCK |
| Timing of MPC command to POWER                                      | tMPCPDEN | tMPC_delay                                |                                     | tMPC_delay                                |                                     | tMPC_delay                                |                                     | nCK |

|                                                                              |                  |                                    |                   |                                    |                   |      |                   |     |
|------------------------------------------------------------------------------|------------------|------------------------------------|-------------------|------------------------------------|-------------------|------|-------------------|-----|
| DOWN ENTRY command                                                           |                  |                                    |                   |                                    |                   |      |                   |     |
| <b>MPC Command Timing</b>                                                    |                  |                                    |                   |                                    |                   |      |                   |     |
| MPC to any other valid command                                               | tMPC_Delay       | tMRD                               |                   | tMRD                               |                   | tMRD |                   | nCK |
| Time between stable MPC command and first falling CS edge (setup)            | tMC_MPC_Setup    | 3                                  |                   | 3                                  |                   | 3    |                   | nCK |
| Time between first rising CS edge and stable MPC command (HOLD)              | tMC_MPC_Hold     | 3                                  |                   | 3                                  |                   | 3    |                   | nCK |
| Time CS_n is held LOW to register MPC command                                | tMPC_CS          | 3.5                                | 8                 | 3.5                                | 8                 | 3.5  | 8                 | nCK |
| <b>PDA Timing</b>                                                            |                  |                                    |                   |                                    |                   |      |                   |     |
| PDA ENUMERATE ID command to any other command cycle                          | tPDA_DELAY       | tPDA_DQS_DELAY (MAX) + BL/2 + 19ns |                   | tPDA_DQS_DELAY (MAX) + BL/2 + 19ns |                   | TBD  |                   | ns  |
| Delay to rising strobe edge used for sampling DQ during PDA operation        | tPDA_DQS_DELAY   | 5                                  | 18                | 5                                  | 18                | TBD  | TBD               | ns  |
| DQS setup time during PDA operation                                          | tPDA_S           | 3                                  |                   | 3                                  |                   | TBD  |                   | nCK |
| DQS hold time during PDA operation                                           | tPDA_H           | 3                                  |                   | 3                                  |                   | TBD  |                   | nCK |
| <b>Read Training Timing</b>                                                  |                  |                                    |                   |                                    |                   |      |                   |     |
| Registration of MRW continuous burst mode exit to next valid command delay   | tCont_Exit_Delay |                                    | tCont_Exit + tMRW |                                    | tCont_Exit + tMRW |      | tCont_Exit + tMRW | ns  |
| Registration of MRW continuous burst mode exit to end of training mode       | tCont_Exit       |                                    | CL+BL/2+10nCK     |                                    | CL+BL/2+10nCK     |      | CL+BL/2+10nCK     | ns  |
| <b>Read Preamble Timing</b>                                                  |                  |                                    |                   |                                    |                   |      |                   |     |
| Delay from MRW command to DQS driven                                         | tSDOn            |                                    | 12nCK, 20ns (MAX) |                                    | 12nCK, 20ns (MAX) |      | 12nCK, 20ns (MAX) |     |
| Delay from MRW command to DQS disabled                                       | tSDOff           |                                    | 12nCK, 20ns (MAX) |                                    | 12nCK, 20ns (MAX) |      | 12nCK, 20ns (MAX) |     |
| <b>CA Training Mode Timing</b>                                               |                  |                                    |                   |                                    |                   |      |                   |     |
| Registration of CAM entry command to start of training samples time          | tCATM_Entry      | 20                                 |                   | 20                                 |                   | 20   |                   | ns  |
| Registration of CATM exit CS_n assertion to end of training mode (when DQ is | tCATM_Exit       |                                    | 14                |                                    | 14                |      | 14                | ns  |

|                                                                                                                                      |                                 |      |     |      |     |      |     |     |
|--------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------|-----|------|-----|------|-----|-----|
| no longer driven by the device).                                                                                                     |                                 |      |     |      |     |      |     |     |
| Registration of CATM exit to next valid command delay                                                                                | tCATM_Exit_Delay                | 20   |     | 20   |     | 20   |     | ns  |
| Time from sample evaluation to output on DQ bus                                                                                      | tCATM_Valid                     |      | 20  |      | 20  |      | 20  | ns  |
| Time output is available on DQ bus                                                                                                   | tCATM_DQ_Window                 | 2    |     | 2    |     | 2    |     | nCK |
| CS_n assertion duration to exit CATM                                                                                                 | tCATM_CS_Exit                   | 2    | 8   | 2    | 8   | 2    | 8   | nCK |
| Registration of CSTM entry command to start of training samples time                                                                 | tCSTM_Entry                     | 20   |     | 20   |     | 20   |     | ns  |
| Min time between last CS_n pulse and first pulse of MPC command to exit CSTM                                                         | tCSTM_Min_to_MPC_exit           | 4    |     | 4    |     | 4    |     | nCK |
| Registration of CSTM exit command to end of training mode                                                                            | tCSTM_Exit                      |      | 20  |      | 20  |      | 20  | ns  |
| Time from sample evaluation to output on DQ bus                                                                                      | tCSTM_Valid                     |      | 20  |      | 20  |      | 20  | ns  |
| Time output is available on DQ bus                                                                                                   | tCSTM_DQ_Window                 | 2    |     | 2    |     | 2    |     | nCK |
| Registration of CSTM exit to next valid command delay                                                                                | tCSTM_Exit_Delay                | 20   |     | 20   |     | 20   |     | ns  |
| <b>Write Leveling Timing</b>                                                                                                         |                                 |      |     |      |     |      |     |     |
| Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid | tWLPEN                          | 0    | 15  | 0    | 15  | 0    | 15  | ns  |
| Write leveling output delay                                                                                                          | tWLO                            | 0    | 9.5 | 0    | 9.5 | 0    | 9.5 | ns  |
| Write leveling output error                                                                                                          | tWLOE                           | 0    | 2   | 0    | 2   | 0    | 2   | ns  |
| Width of write leveling internal pulse                                                                                               | tWL_Pulse_Width                 | 2    |     | 2    |     | 2    |     | tCK |
| <b>VREFCA/VREFCS Timing</b>                                                                                                          |                                 |      |     |      |     |      |     |     |
| VREFCA/VREFCS command to any other valid command delay                                                                               | tVREFCA_Delay/<br>tVREFCS_Delay | tMRD |     | tMRD |     | tMRD |     | nCK |
| Time CS_n is held LOW to register VREFCA/VREFCS                                                                                      | tVREFCA_CS/<br>tVREFCS_CS       | 3.5  | 8   | 3.5  | 8   | 3.5  | 8   | nCK |

|                                                                       |                  |                                         |    |                           |    |                           |    |     |
|-----------------------------------------------------------------------|------------------|-----------------------------------------|----|---------------------------|----|---------------------------|----|-----|
| command                                                               |                  |                                         |    |                           |    |                           |    |     |
| hPPR/sPPR Timing                                                      |                  |                                         |    |                           |    |                           |    |     |
| hPPR programming time (x4/x8)                                         | tPGMa            | 1000                                    |    | 1000                      |    | 1000                      |    | ms  |
| hPPR programming time (x16)                                           | tPGMb            | 2000                                    |    | 2000                      |    | 2000                      |    | ms  |
| sPPR programming time                                                 | tPGM_sPPR        | CWL +8tCK +tWR                          |    | CWL +8tCK +tWR            |    | CWL +8tCK +tWR            |    | tCK |
| hPPR/sPPR recognition time                                            | tPGM_Exit        | tRP                                     |    | tRP                       |    | tRP                       |    | ns  |
| hPPR program exit and new address setting time                        | tPGMPST          | 50                                      |    | 50                        |    | 50                        |    | μs  |
| sPPR program exit and new address setting time                        | tPGMPST_sP<br>PR | tMRD                                    |    | tMRD                      |    | tMRD                      |    | ns  |
| DQS Interval Oscillator Readout Timing                                |                  |                                         |    |                           |    |                           |    |     |
| Delay time from DQS interval oscillator stop to mode register readout | tOSCO            | tMPC_De<br>lay                          |    | tMPC_De<br>lay            |    | tMPC_De<br>lay            |    | nCK |
| DQS interval oscillator start gap in automatic stop mode              | tOSCS            | tMPC_Delay + DQS interval timer runtime |    |                           |    |                           |    | nCK |
| ECS Timing                                                            |                  |                                         |    |                           |    |                           |    |     |
| ECS operation time                                                    | tECSc            | 176nCK,<br>110ns<br>(MAX)               |    | 176nCK,<br>110ns<br>(MAX) |    | 176nCK,<br>110ns<br>(MAX) |    |     |
| CRC Error Reporting Timing                                            |                  |                                         |    |                           |    |                           |    |     |
| CRC error to ALERT_n_latency                                          | tCRC_ALERT       | 3                                       | 13 | 3                         | 13 | 3                         | 13 | ns  |
| CRC ALERT_n pulse width                                               | CRC_ALERT_<br>PW | 12                                      | 20 | 12                        | 20 | 12                        | 20 | nCK |

## 10. SPD

| Byte Number | Function Described                                                                    | Hex Value |
|-------------|---------------------------------------------------------------------------------------|-----------|
| 0           | Number of Bytes in SPD Device                                                         | 30        |
| 1           | SPD Revision for Base Configuration Parameters                                        | 10        |
| 2           | Key Byte / Host Bus Command Protocol Type                                             | 12        |
| 3           | Key Byte / Module Type                                                                | 02        |
| 4           | First SDRAM Density and Package                                                       | 04        |
| 5           | First SDRAM Addressing                                                                | 00        |
| 6           | First SDRAM I/O Width                                                                 | 40        |
| 7           | First SDRAM Bank Groups & Banks Per Bank Group                                        | 42        |
| 8           | Second SDRAM Density and Package                                                      | 00        |
| 9           | Second SDRAM Addressing                                                               | 00        |
| 10          | Second SDRAM I/O Width                                                                | 00        |
| 11          | Second SDRAM Bank Groups & Banks Per Bank Group                                       | 00        |
| 12          | SDRAM BL32 & Post Package Repair                                                      | A0        |
| 13          | SDRAM Duty Cycle Adjuster & Partial Array Self Refresh                                | 01        |
| 14          | SDRAM Fault Handling                                                                  | 07        |
| 15          | Reserved                                                                              | 00        |
| 16          | SDRAM Nominal Voltage, VDD                                                            | 00        |
| 17          | SDRAM Nominal Voltage, VDDQ                                                           | 00        |
| 18          | SDRAM Nominal Voltage, VPP                                                            | 00        |
| 19          | Reserved                                                                              | 00        |
| 20          | SDRAM Minimum Cycle Time ( $t_{CKAVGmin}$ ), Least Significant Byte                   | A0        |
| 21          | SDRAM Minimum Cycle Time ( $t_{CKAVGmin}$ ), Most Significant Byte                    | 01        |
| 22          | SDRAM Maximum Cycle Time ( $t_{CKAVGmax}$ ), Least Significant Byte                   | F2        |
| 23          | SDRAM Maximum Cycle Time ( $t_{CKAVGmax}$ ), Most Significant Byte                    | 03        |
| 24          | CAS Latencies Supported, First Byte                                                   | 7A        |
| 25          | CAS Latencies Supported, Second Byte                                                  | 0D        |
| 26          | CAS Latencies Supported, Third Byte                                                   | 00        |
| 27          | CAS Latencies Supported, Fourth Byte                                                  | 00        |
| 28          | CAS Latencies Supported, Fifth Byte                                                   | 00        |
| 29          | Reserved                                                                              | 00        |
| 30          | SDRAM Minimum CAS Latency Time ( $t_{Aamin}$ ), Least Significant Byte                | 80        |
| 31          | SDRAM Minimum CAS Latency Time ( $t_{Aamin}$ ), Most Significant Byte                 | 3E        |
| 32          | SDRAM Minimum RAS to CAS Delay Time ( $t_{RCDmin}$ ), Least Significant Byte          | 80        |
| 33          | SDRAM Minimum RAS to CAS Delay Time ( $t_{RCDmin}$ ), Most Significant Byte           | 3E        |
| 34          | SDRAM Minimum Row Precharge Delay Time ( $t_{RPmin}$ ), Least Significant Byte        | 80        |
| 35          | SDRAM Minimum Row Precharge Delay Time ( $t_{RPmin}$ ), Most Significant Byte         | 3E        |
| 36          | SDRAM Minimum Active to Precharge Delay Time ( $t_{RASmin}$ ), Least Significant Byte | 00        |

|    |                                                                                                                       |    |
|----|-----------------------------------------------------------------------------------------------------------------------|----|
| 37 | SDRAM Minimum Active to Precharge Delay Time ( $t_{RASmin}$ ), Most Significant Byte                                  | 7D |
| 38 | SDRAM Minimum Active to Active/Refresh Delay Time ( $t_{RCmin}$ ), Least Significant Byte                             | 80 |
| 39 | SDRAM Minimum Active to Active/Refresh Delay Time ( $t_{RCmin}$ ), Most Significant Byte                              | BB |
| 40 | SDRAM Minimum Write Recovery Time ( $t_{WRmin}$ ), Least Significant Byte                                             | 30 |
| 41 | SDRAM Minimum Write Recovery Time ( $t_{WRmin}$ ), Most Significant Byte                                              | 75 |
| 42 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFC1min}$ , $t_{RFC1slr min}$ ), Least Significant Byte               | 27 |
| 43 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFC1min}$ , $t_{RFC1slr min}$ ), Most Significant Byte                | 01 |
| 44 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFC2min}$ , $t_{RFC2slr min}$ ), Least Significant Byte               | A0 |
| 45 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFC2min}$ , $t_{RFC2slr min}$ ), Most Significant Byte                | 00 |
| 46 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFCsbmin}$ , $t_{RFCsb slr min}$ ), Least Significant Byte            | 82 |
| 47 | SDRAM Minimum Refresh Recovery Delay Time ( $t_{RFCsb dlr min}$ ), Most Significant Byte                              | 00 |
| 48 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFC1 dlr min}$ ), Least Significant Byte  | 00 |
| 49 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFC1 dlr min}$ ), Most Significant Byte   | 00 |
| 50 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFC2 dlr min}$ ), Least Significant Byte  | 00 |
| 51 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFC2 dlr min}$ ), Most Significant Byte   | 00 |
| 52 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFCsb dlr min}$ ), Least Significant Byte | 00 |
| 53 | SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank ( $t_{RFCsb dlr min}$ ), Most Significant Byte  | 00 |
| 54 | SDRAM Refresh Management, First Byte, First SDRAM                                                                     | D4 |
| 55 | SDRAM Refresh Management, Second Byte, First SDRAM                                                                    | 00 |
| 56 | SDRAM Refresh Management, First Byte, Second SDRAM                                                                    | 00 |
| 57 | SDRAM Refresh Management, Second Byte, Second SDRAM                                                                   | 00 |
| 58 | SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM                                                    | D4 |
| 59 | SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM                                                   | 00 |
| 60 | SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM                                                   | 00 |
| 61 | SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM                                                  | 00 |
| 62 | SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM                                                    | D4 |
| 63 | SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM                                                   | 00 |
| 64 | SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM                                                   | 00 |
| 65 | SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM                                                  | 00 |
| 66 | SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM                                                    | D4 |
| 67 | SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM                                                   | 00 |
| 68 | SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM                                                   | 00 |
| 69 | SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM                                                  | 00 |
| 70 | SDRAM Minimum Active to Active Command Delay Time, Same Bank Group ( $t_{RRD_Lmin}$ ), Least Significant Byte         | 88 |

|         |                                                                                                                                                                           |    |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| 71      | SDRAM Minimum Active to Active Command Delay Time, Same Bank Group ( $t_{RRD\_Lmin}$ ), Most Significant Byte                                                             | 13 |
| 72      | SDRAM Minimum Active to Active Command Delay Time, Same Bank Group ( $t_{RRD\_Lmin}$ ), Lower Clock Limit                                                                 | 08 |
| 73      | SDRAM Minimum CAS <sub>n</sub> to CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_Lmin}$ ), Least Significant Byte                                        | 88 |
| 74      | SDRAM Minimum CAS <sub>n</sub> to CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_Lmin}$ ), Most Significant Byte                                         | 13 |
| 75      | SDRAM Minimum CAS <sub>n</sub> to CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_Lmin}$ ), Lower Clock Limit                                             | 08 |
| 76      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_L\_WRmin}$ ), Least Significant Byte                        | 20 |
| 77      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_L\_WRmin}$ ), Most Significant Byte                         | 4E |
| 78      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Same Bank Group ( $t_{CCD\_L\_WRmin}$ ), Lower Clock Limit                             | 20 |
| 79      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Second Write not RMW, Same Bank Group ( $t_{CCD\_L\_WR2min}$ ), Least Significant Byte | 10 |
| 80      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Second Write not RMW, Same Bank Group ( $t_{CCD\_L\_WR2min}$ ), Most Significant Byte  | 27 |
| 81      | SDRAM Minimum Write CAS <sub>n</sub> to Write CAS <sub>n</sub> Command Delay Time, Second Write not RMW, Same Bank Group ( $t_{CCD\_L\_WR2min}$ ), Lower Clock Limit      | 10 |
| 82      | SDRAM Minimum Four Activate Window ( $t_{FAWmin}$ ), Least Significant Byte                                                                                               | 15 |
| 83      | SDRAM Minimum Four Activate Window ( $t_{FAWmin}$ ), Most Significant Byte                                                                                                | 34 |
| 84      | SDRAM Minimum Four Activate Window ( $t_{FAWmin}$ ), Lower Clock Limit                                                                                                    | 20 |
| 85      | SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, ( $t_{WTR\_Lmin}$ ), Least Significant Byte                                                     | 10 |
| 86      | SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, ( $t_{WTR\_Lmin}$ ), Most Significant Byte                                                      | 27 |
| 87      | SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, ( $t_{WTR\_Lmin}$ ), Lower Clock Limit                                                          | 10 |
| 88      | SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, ( $t_{WTR\_Smin}$ ), Least Significant Byte                                                | C4 |
| 89      | SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, ( $t_{WTR\_Smin}$ ), Most Significant Byte                                                 | 09 |
| 90      | SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, ( $t_{WTR\_Smin}$ ), Lower Clock Limit                                                     | 04 |
| 91      | SDRAM Minimum Internal Read to Precharge Command Delay Time, ( $t_{RTPmin}$ ), Least Significant Byte                                                                     | 4C |
| 92      | SDRAM Minimum Internal Read to Precharge Command Delay Time, ( $t_{RTPmin}$ ), Most Significant Byte                                                                      | 1D |
| 93      | SDRAM Minimum Internal Read to Precharge Command Delay Time, ( $t_{RTPmin}$ ), Lower Clock Limit                                                                          | 0C |
| 94~127  | Reserved -- must be coded as 0x00                                                                                                                                         | 00 |
| 128~191 | Reserved for future use                                                                                                                                                   | 00 |
| 192     | SPD Revision for SPD bytes 192~447                                                                                                                                        | 10 |
| 193     | Hashing Sequence                                                                                                                                                          | 00 |
| 194     | SPD Manufacturer ID Code, First Byte                                                                                                                                      | 80 |
| 195     | SPD Manufacturer ID Code, Second Byte                                                                                                                                     | B3 |
| 196     | SPD Device Type                                                                                                                                                           | 80 |
| 197     | SPD Device Revision Number                                                                                                                                                | 21 |

|         |                                                  |       |
|---------|--------------------------------------------------|-------|
| 198     | PMIC 0 Manufacturer ID Code, First Byte          | 80    |
| 199     | PMIC 0 Manufacturer ID Code, Second Byte         | B3    |
| 200     | PMIC 0 Device Type                               | 82    |
| 201     | PMIC 0 Revision Number                           | 20    |
| 202     | PMIC 1 Manufacturer ID Code, First Byte          | 00    |
| 203     | PMIC 1 Manufacturer ID Code, Second Byte         | 00    |
| 204     | PMIC 1 Device Type                               | 00    |
| 205     | PMIC 1 Revision Number                           | 00    |
| 206     | PMIC 2 Manufacturer ID Code, First Byte          | 00    |
| 207     | PMIC 2 Manufacturer ID Code, Second Byte         | 00    |
| 208     | PMIC 2 Device Type                               | 00    |
| 209     | PMIC 2 Revision Number                           | 00    |
| 210     | Thermal Sensor Manufacturer ID Code, First Byte  | 00    |
| 211     | Thermal Sensor Manufacturer ID Code, Second Byte | 00    |
| 212     | Thermal Sensor Device Type                       | 00    |
| 213     | Thermal Sensor Revision Number                   | 00    |
| 214     | DRAM Specification Level                         | 00    |
| 215     | SPD Specification Level                          | 00    |
| 216     | PMIC0 Specification Level                        | 00    |
| 217     | PMIC1 Specification Level                        | 00    |
| 218     | PMIC2 Specification Level                        | 00    |
| 219     | TS Specification Level                           | 00    |
| 220     | DIMM Specification Level                         | 00    |
| 221~229 | Reserved                                         | 00    |
| 230     | Module Nominal Height                            | 11    |
| 231     | Module Maximum Thickness                         | 01    |
| 232     | Reference Raw Card Used                          | 02    |
| 233     | DIMM Attributes                                  | 71    |
| 234     | Module Organization                              | 00    |
| 235     | Memory Channel Bus Width                         | 22    |
| 236~239 | Reserved                                         | 00    |
| 240~447 | Reserved                                         | 00    |
| 448~509 | Reserved for future use                          | 00    |
| 510~511 | CRC for SPD bytes 0~509                          | D4 03 |
| 512     | Module Manufacturer ID Code, First Byte          | 8A    |
| 513     | Module Manufacturer ID Code, Second Byte         | C8    |
| 514     | Module Manufacturing Location                    | 02    |
| 515~516 | Module Manufacturing Date                        | -     |
| 517~520 | Module Serial Number                             | -     |

|          |                                        |                                                                                                       |
|----------|----------------------------------------|-------------------------------------------------------------------------------------------------------|
| 521~550  | Module Part Number                     | 53 51 52 2D 55 44<br>35 4E 38 47 34 4B<br>38 4D 4E 47 41 42<br>20 20 20 20 20 20<br>20 20 20 20 20 20 |
| 551      | Module Revision Code                   | 00                                                                                                    |
| 552      | DRAM Manufacturer ID Code, First Byte  | 80                                                                                                    |
| 553      | DRAM Manufacturer ID Code, Second Byte | 2C                                                                                                    |
| 554      | DRAM Stepping                          | 00                                                                                                    |
| 555~639  | Manufacturer's Specific Data           | -                                                                                                     |
| 640~703  | End User Programmable                  | 00                                                                                                    |
| 704~767  | End User Programmable                  | 00                                                                                                    |
| 768~831  | End User Programmable                  | 00                                                                                                    |
| 832~895  | End User Programmable                  | 00                                                                                                    |
| 896~959  | End User Programmable                  | 00                                                                                                    |
| 960~1023 | End User Programmable                  | 00                                                                                                    |

**Appendix: Part Number Table**

| Product                                   | Advantech PN              |
|-------------------------------------------|---------------------------|
| SGRAM 8GB U-DDR5-4800 1Gx16 Micron (0~85) | <b>SQR-UD5N16G4K8MNAB</b> |