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3D NAND Flash with Advanced ECC Technology for Industrial Application

With the evolutionary pace of technology and the constant pursuit of ever greater performance, non-volatile storage and NAND flash have gradually become the mainstream storage media types in the IT market. To achieve faster performance, ultra-scalability, and better cost efficiency, advanced 3D NAND flash technology was introduced onto the market by flash manufacturers in recent years.

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Introduction

With the evolutionary pace of technology and the constant pursuit of ever greater performance, non-volatile storage and NAND flash have gradually become the mainstream storage media types in the IT market. To achieve faster performance, ultra-scalability, and better cost efficiency, advanced 3D NAND flash technology was introduced onto the market by flash manufacturers in recent years. However, for industrial grade NAND flash storage applications, finding the right balance of both performance and reliability is crucial.

The purpose of this paper is to provide an overview of NAND flash management technology. The first section gives a brief overview of NAND flash types, including SLC, MLC, TLC, and 3D TLC (BiCS3), and comparisons of their performance and endurance. The later sections introduce how Advantech SQFlash NAND flash management technology enhances storage devices to meet the dual demands for high capacity and high performance, as well as industrial grade reliability. This includes the introduction of advanced Error Correcting Code (ECC) technology, low-density parity-check (LDPC) code, for endurance, and reliability improvements.

NAND Flash Type

Common NAND Flash

NAND flash types are commonly referred to as single-level cell (SLC), multi-level cell (MLC), and triple-level cell (TLC). These three types are all planar NAND flash. The basic operating concept is as shown in Figure 1. Each cell consists of a single transistor and a floating gate, which is located between the gate and source/drain and allows electrons to be stored inside. For SLC flash, one bit data can be stored to each cell at a time, and there are two states for each cell, 0 and 1. As for MLC flash, two bits could be stored to each cell at a time and there are four states for each cell (00 to 11). In terms of TLC, 3 bits can be stored to each cell at a time and there are eight states for each cell (000 to 111). Cell states are determined by the threshold voltage (V_t) of each cell, and the voltage is an interpretation of the amount of charge stored inside the floating gate, as shown in Figure 2.

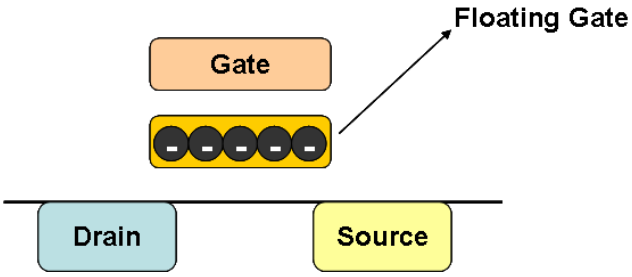

Figure 1: Basic Structure of a Memory Cell

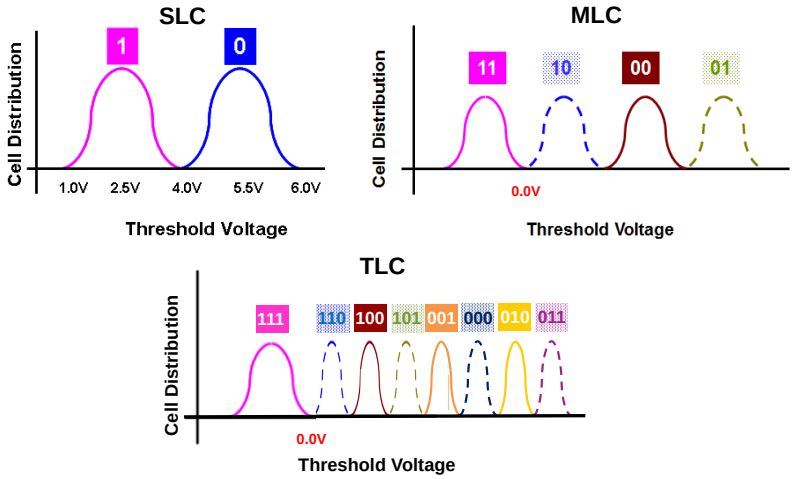

Figure 2: Cell Distribution vs. Threshold Voltage for SLC, MLC and TLC

Since TLC flash cells store more bits than MLC and SLC, TLC provides higher density for lower bit-cost. However, the tradeoff for cost-saving is greater

power consumption and lower endurance, due to more voltage levels required and technology limitations as Table 1 shows. In industrial grade storage devices, SLC and MLC are often used due to higher endurance and reliability requirements. Whereas, TLC flash tends to be used more in commercial applications.

Flash Type	SLC	MLC	TLC
Storage	1 bits / cell	2 bits / cell	3 bits / cell
Program / Erase Cycle (BCH)	100,000+	3,000+	500 ~ 1,000
Write Performance	Highest	High	Low
Cost-per-bit	Highest	High	Low
Density	Lowest	Middle	High
Power Consumption	Lowest	Middle	Highest

Table 1: Feature Comparison of Common NAND Flash Type

3D NAND Flash

In recent years, due to the increasing demand for data storage in order to achieve higher storage density and lower bit-cost, NAND flash manufacturers have introduced their own three dimensional (3D) NAND flash technology. This paper will describe Toshiba 3D NAND flash, Bit-Cost Scalable (BiCS), in detail.

NAND flash uses floating-gate transistors to store electrons. To manage and store more data, several transistors are connected in series known as a NAND string. The bit line is pulled low when all the word lines are pulled high above the transistors' V_t. Figure 3 shows the structure of planar NAND flash.

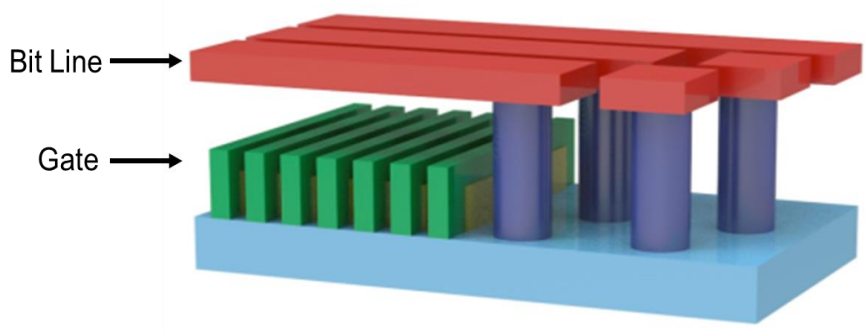

Figure 3: Structure of Planar NAND Flash

3D NAND flash technology is a precise process of vertically integrating NAND strings. The NAND strings are connected vertically in a series, and the memory transistors change from floating-gate types to trapped charge types. The BiCS 3D NAND Flash architecture is described in Figure 4. The first element of the architecture is the control gate stack shown by the different rectangle elements piled on top of each other, whereas the bottom rectangle plate is the source line terminating the flash strings. Multiple holes are drilled through the stacks and filled with poly-silicon in order to form a series of vertically-arranged NAND Flash memory cells. Bit Lines are on top of the structure. The control gate plate intersection with a pillar maps a single memory cell. Each NAND Flash string of cells is connected to a bit line, whereas the bottom of the string is connected to a common source diffusion layer formed directly on the process substrate made of silicon. The overall storage capacity and the bit density of the memory can be increased by adding control gate plates.

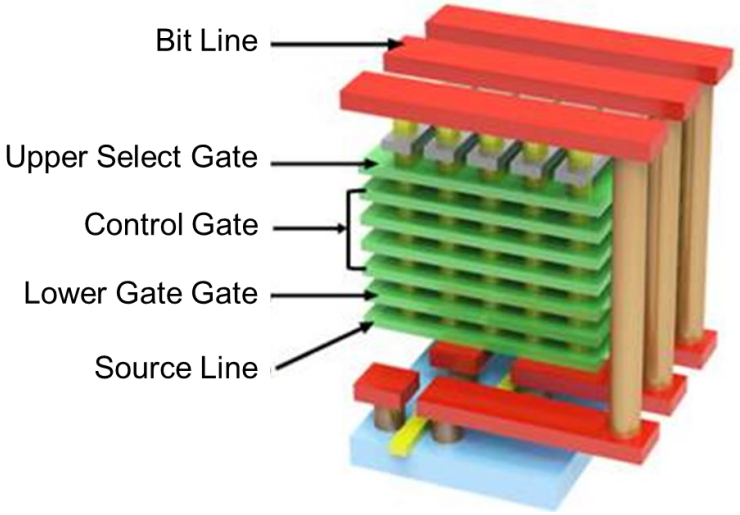

Figure 4: Structure of BiCS 3D NAND Flash

3D NAND technology breaks the limitations of planar NAND processing by vertically stacking. By stacking more layers, 3D NAND can increase the unit density of storage. Currently, NAND Flash manufacturers can already provide up to 64 layers of 3D NAND (Toshiba BiCS3) and continue to develop more layers. In addition to the higher storage density of 3D NAND (due to the increased density of each cell), faster read and write performance can be achieved through simple algorithms, and better reliability can be provided by reducing cell-to-cell program interference, meaning reduced power loss and lower overall cost.

Flash Type	Planar NAND Flash			3D NAND
	SLC	MLC	TLC	BiCS3 (3D TLC)
Storage	1 bit / cell	2 bits / cell	3 bits / cell	3 bits / cell
Program / Erase Cycle (BCH)	100,000+	3,000+	500 ~ 1,000	1,000 ~ 1,500
Write Performance	Highest	High	Low	Middle
Cost-per-bit	Highest	High	Low	Lowest
Density	Lowest	Middle	High	Highest
Power Consumption	Lowest	Middle	Highest	High

Table 2: Feature Comparison of All NAND Flash types

NOTE: If using LDPC as ECC, the P/E cycle of BiCS3 can be up to 3000+ (see "P/E Cycle Experiments of LDPC and BCH" section).

Error Correction Code Technology

BCH and LDPC

For precise data, engineers apply Error Correction Code (ECC) technology to ensure the accuracy of data. As unit density of storage and the numbers of levels of a NAND flash cell increase, the reliability of data with TLC and 3D NAND flash may reduce. So it is necessary to use higher performance ECC technology.

Currently, there are two kinds of ECC: Bose, Chaudhuri, and Hocquenghem (BCH), and Low-Density Parity-Check (LDPC), which are widely used in NAND flash storage. BCH is a traditional algebraic coding method, commonly using bounded-distance decoding and can correct up to a specified, fixed number of errors. Unlike these traditional codes, it can be used for BCH codes to guarantee a specified number of correctable errors.

LDPC codes are especially suitable for NAND flash memories, because of its ability to process both hard-bit (binary) and soft-bit (probabilities of bits) information. An LDPC decoder not only corrects errors by using hard-bit information, but it also uses soft-bit information to correct errors. Therefore, LDPC has excellent performance when both soft-bit and hard-bit information are available. NAND flash memories can be accessed to get both hard-bit and soft-bit data, and this information can be passed to the LDPC decoding circuit to detect and correct errors. LDPC allows the correction of more errors for the same data-to-parity bit ratios when compared to other ECC schemes as

Table 3 shows.

Item	BCH	LDPC
Decoding Algorithm	Algebraic Based	Probability Based
Guaranteed Correction Strength	Yes	No
Performance of Hard bit Decode	Fixed	1.3X BCH
Performance of Soft bit decode	-	2X~3X than BCH
Decoding Complexity	Low	Mid
Die Cost	Low	High

Table 3: BCH and LDPC Comparison

P/E Cycle Experiments of LDPC and BCH

In order to compare the correctable error bit recovery capabilities of LDPC and BCH we need to look at the differences in P/E cycles.

BiCS3 was used for this experiment and the results are shown in Figure 5.

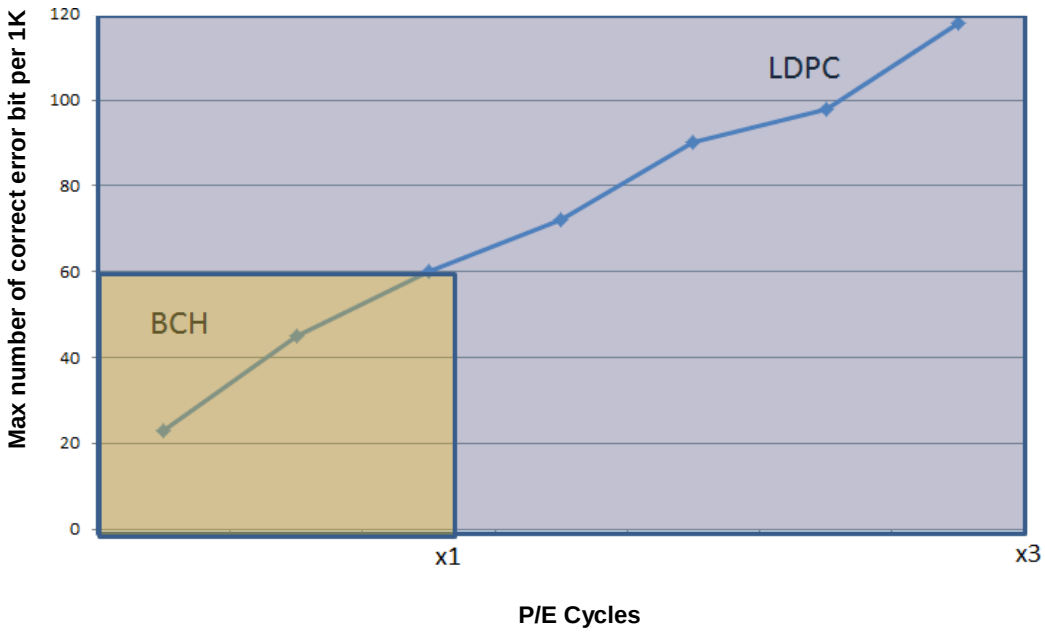

Figure 5: BiCS3 P/E Cycles Experiment

The results indicate that BCH and LDPC both have similar correctable error bits and recovery capability when the P/E cycle is x1. With soft-bit recovery, LDPC provides x3 P/E cycles, which gives excellent correctable error bit

recovery. So LDPC is a highly capable error correction code function for high density NAND storage which helps it to reach higher program/erase cycles with higher correctable error bit recovery. With the ECC capability of LDPC, BiCS3 can boost P/E cycles to over 3,000 times.

Conclusion

In the era of big data and IoT, increasingly more data needs to be stored and accessed. As a result, NAND flash manufacturers continue to develop technologies with higher storage densities in order to be more competitive. From planar NAND flash SLC, MLC, and TLC to 3D NAND flash BiCS3, higher storage density devices have emerged rather quickly in recent years. However, while eager to pursue cost-effectiveness, it is likely that endurance, reliability, and/or performance will be sacrificed. This paper mentions that LDPC ECC technology could enhance the P/E cycle two- or three-fold, which enables 3D NAND flash, BiCS3, to achieve MLC-level endurance. To ensure that customers can meet industrial-grade requirements such as high endurance and high reliability when applying new NAND technology, Advantech SQFlash is continuously conducting R&D on NAND flash management technology to support customer interests.